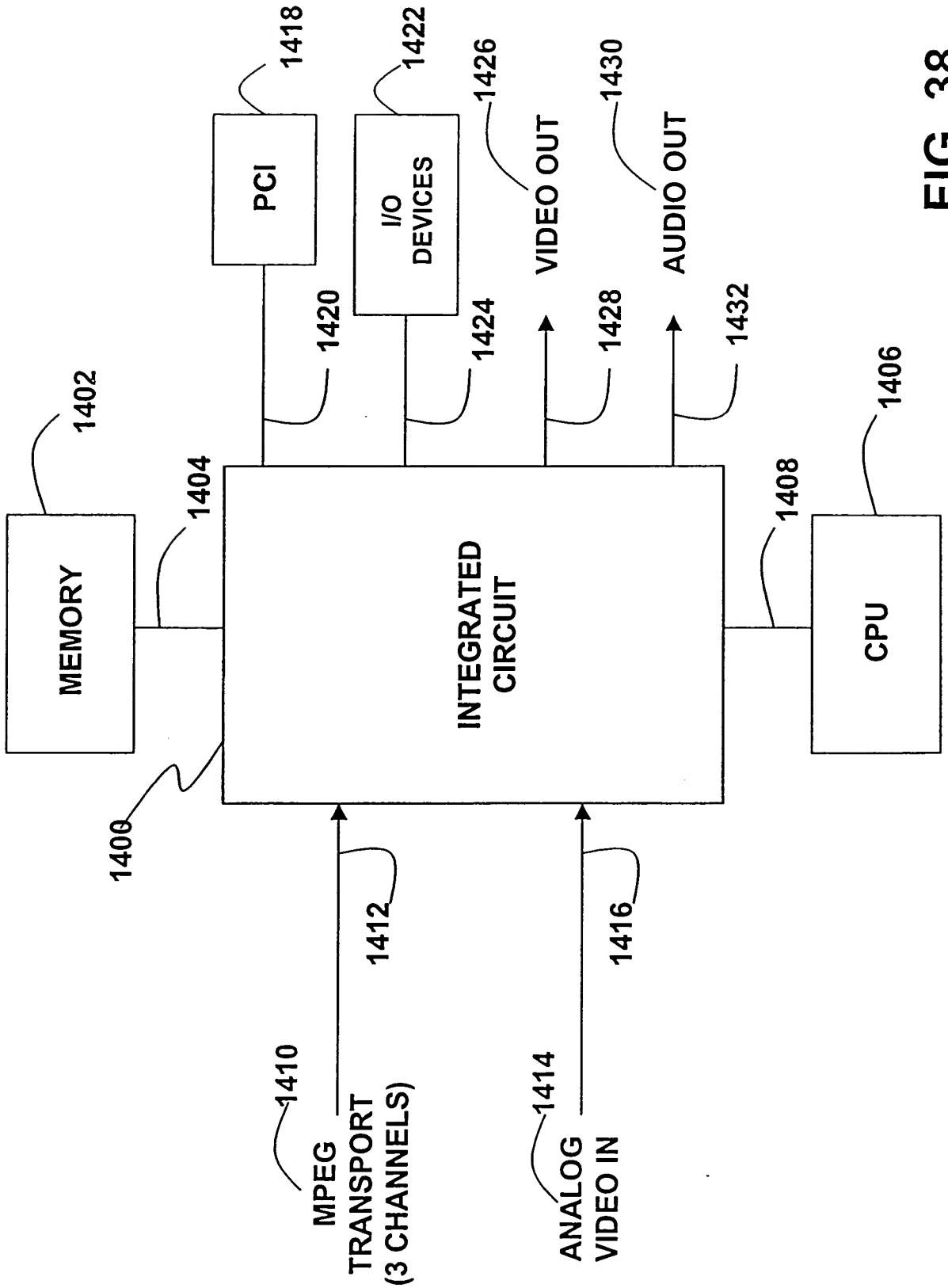
1418
PCI
1422
I/O DEVICES
1426
VIDEO OUT
1430
AUDIO OUT
1420
1424
1428
1432
1402
1404
1406
1408
MEMORY
INTEGRATED CIRCUIT
CPU
1400
1412
1416
1410
MPEG TRANSPORT (3 CHANNELS)
1414
ANALOG VIDEO IN

FIG. 38

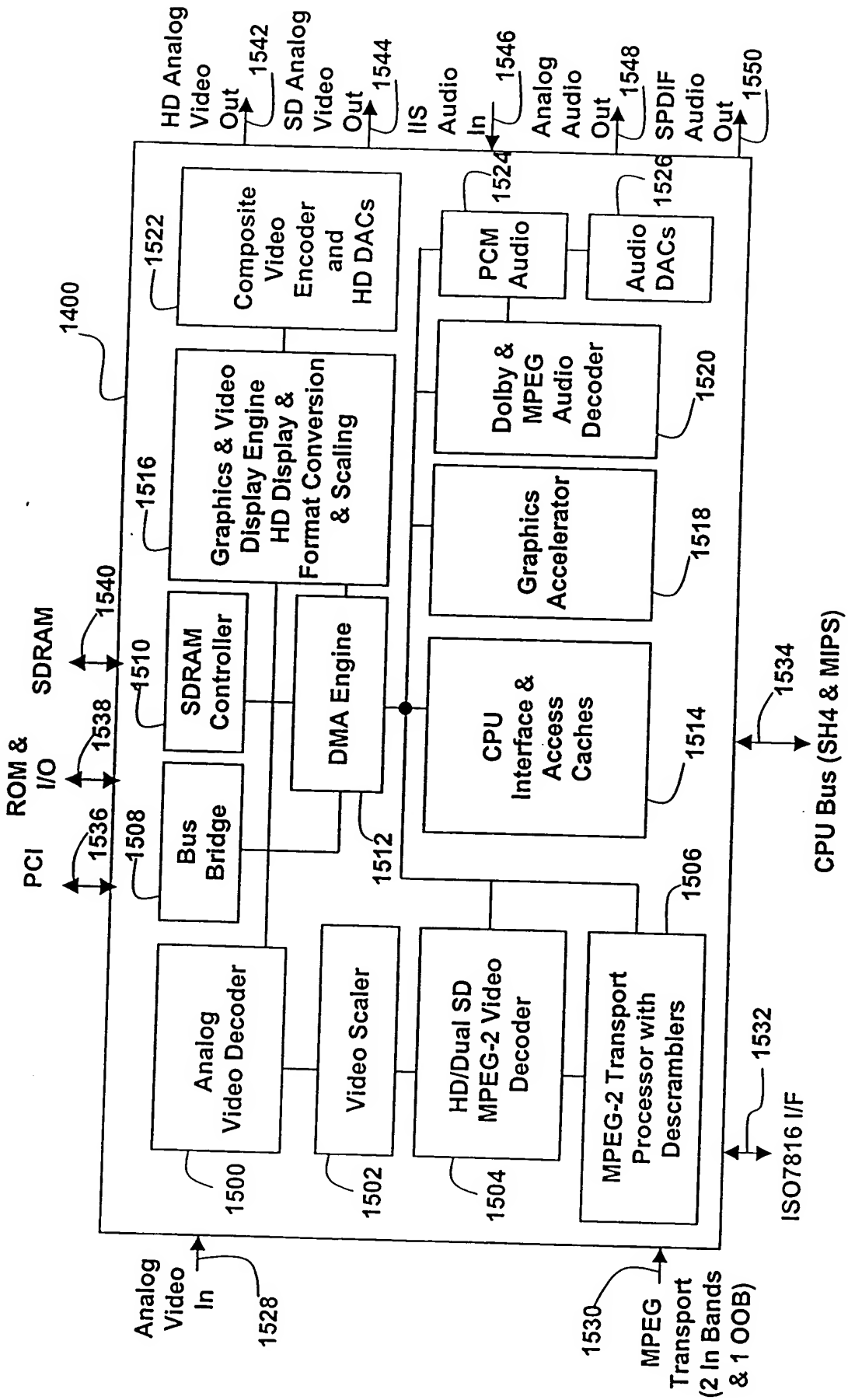
1400
HD Analog Video Out
1542
SD Analog Video Out
1544
IIS Audio In
1546
Analog Audio Out
1548
SPDIF Audio Out
1550
Composite Video Encoder and HD DACs
1522
PCM Audio
1524
Audio DACs
1526
Graphics & Video Display Engine HD Display & Format Conversion & Scaling
1516
Dolby & MPEG Audio Decoder
1520
Graphics Accelerator
1518
SDRAM
1540
SDRAM Controller
1510
DMA Engine
1512
CPU Interface & Access Caches
1514
1534
CPU Bus (SH4 & MIPS)
ROM & I/O
1538
PCI
1536
Bus Bridge
1508
1506
Analog Video Decoder
1500
Video Scaler
1502
HD/Dual SD MPEG-2 Video Decoder
1504
MPEG-2 Transport Processor with Descramblers
1532
ISO7816 I/F
Analog Video In
1528
1530
MPEG Transport (2 In Bands & 1 OOB)

FIG. 39

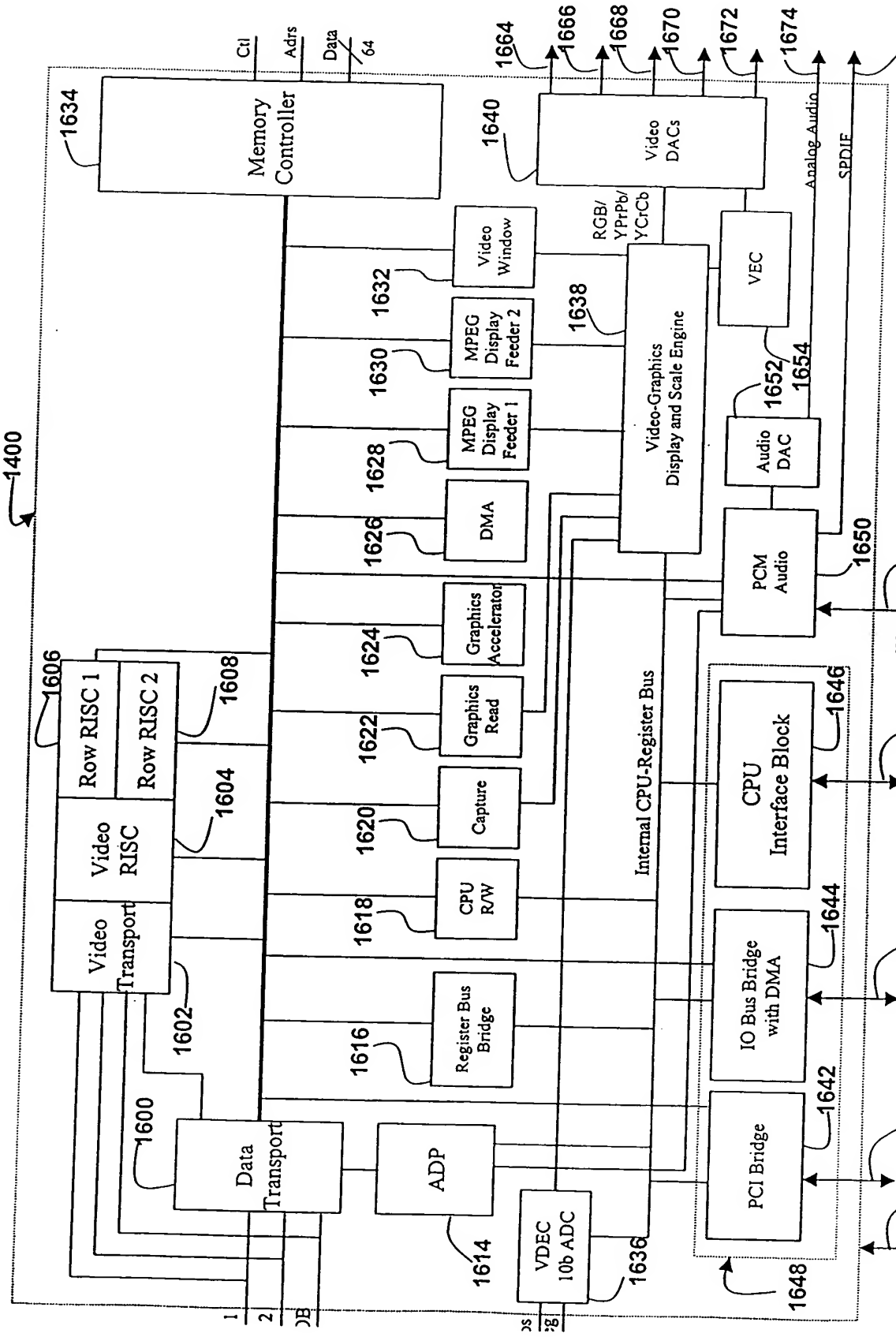
1400
Memory Controller
1634
Ctl
Adrs
Data
64
Video DACs
1640
1664
1666
1668
1670
1672
1674
1676
RGB/ YPrPb/ YCrCb
Analog Audio
SPDIF
Video Window
MPEG Display Feeder 2
MPEG Display Feeder 1
DMA
Graphics Accelerator
Graphics Read
Capture
CPU R/W
Register Bus Bridge
1632
1630
1628
1626
1624
1622
1620
1618
1616
Video-Graphics Display and Scale Engine
1638
VEC
Audio DAC
1652
1654
PCM Audio
1650
IIS Input
1662
Internal CPU-Register Bus
CPU Interface Block
1646
1660
IO Bus Bridge with DMA
1644
1658
PCI Bridge
1642
1656
1678
1648
Row RISC 1
Row RISC 2
1606
1608
Video RISC
1604
Video Transport
1602
Data Transport
1600
ADP
1614
VDEC 10b ADC
1636

FIG. 40

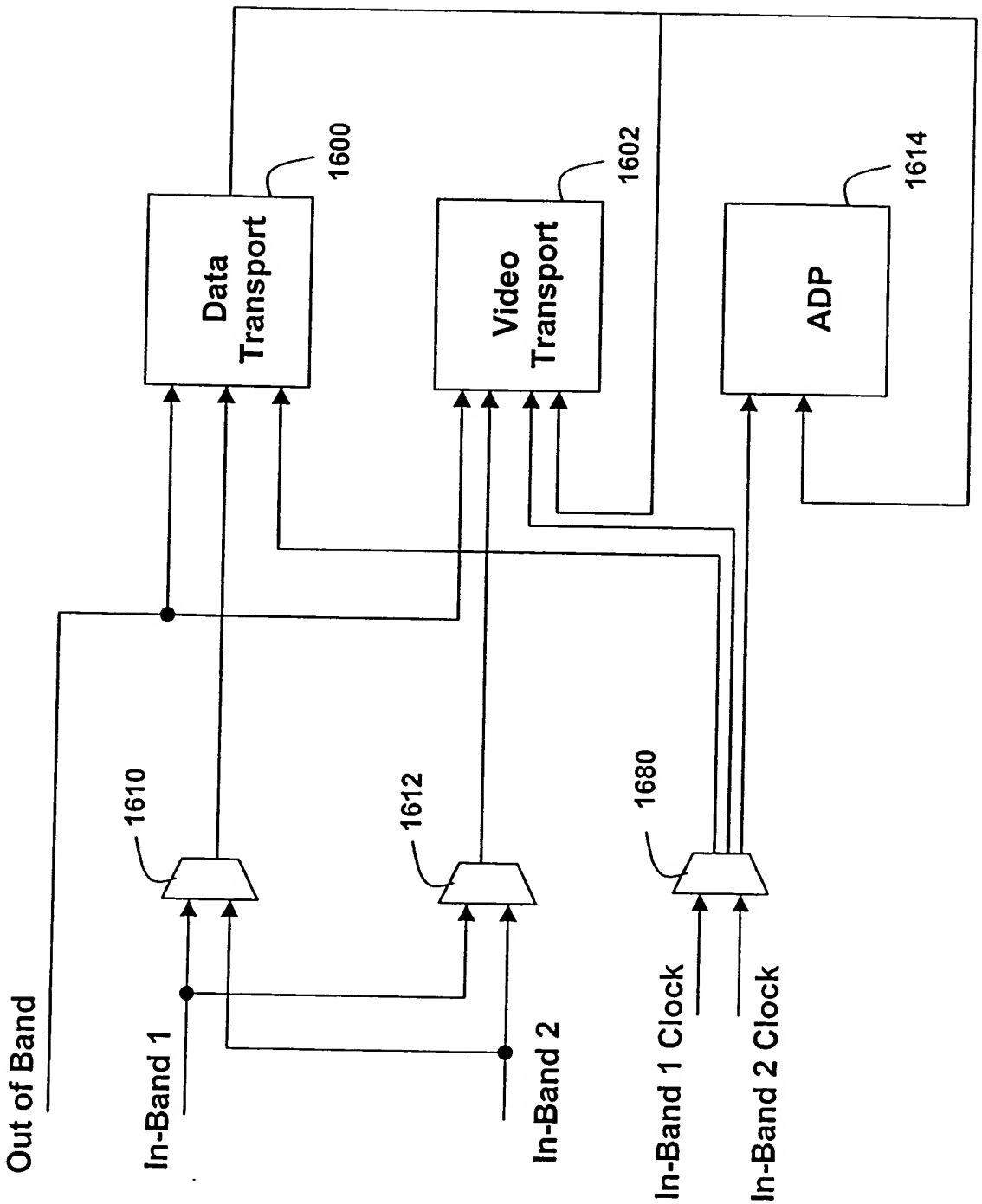
Data Transport
1600
Video Transport
1602
ADP
1614
1610
1612
1680
Out of Band
In-Band 1
In-Band 2
In-Band 1 Clock
In-Band 2 Clock

FIG. 41

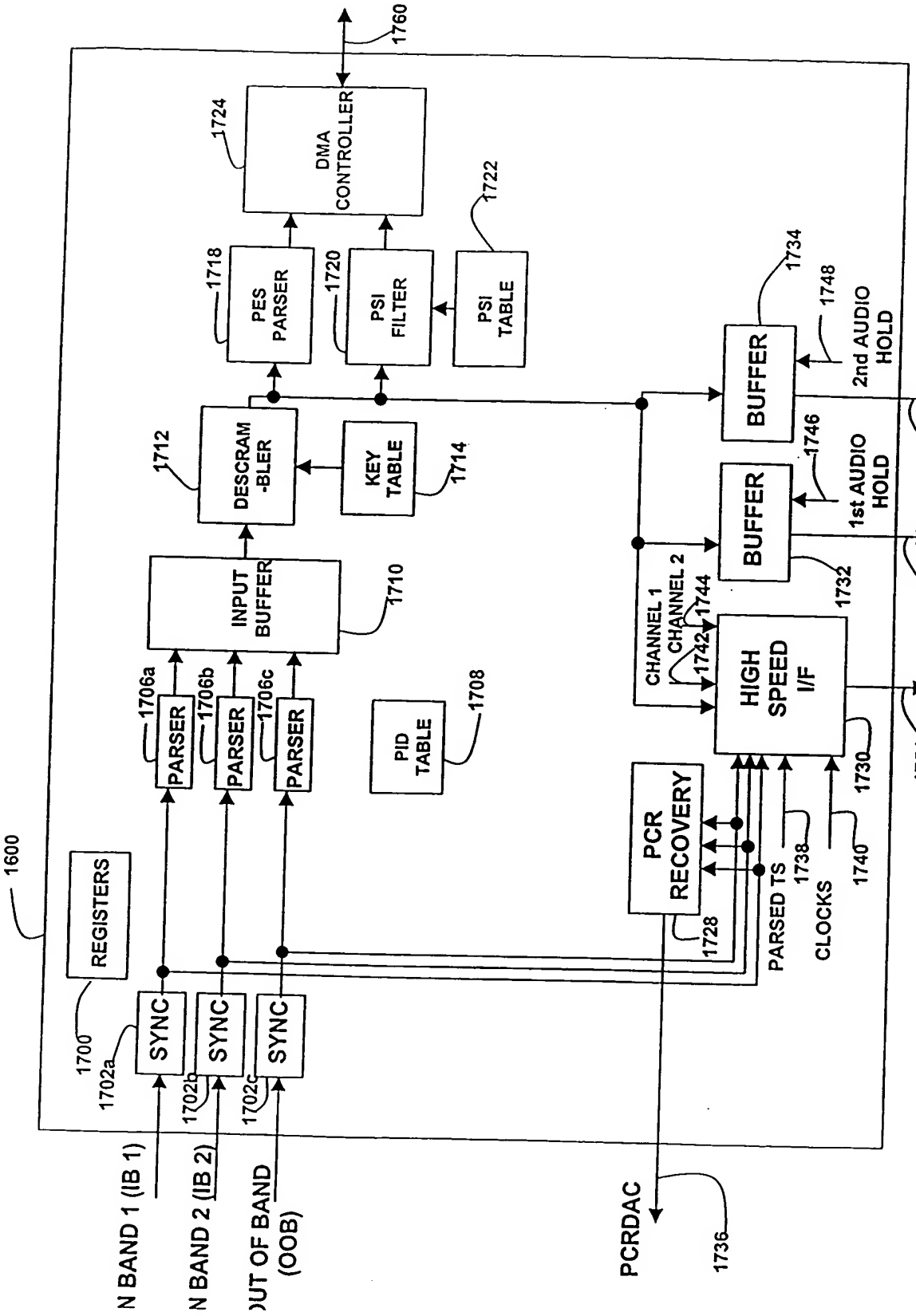
1600
1760
DMA CONTROLLER
1724
PES PARSER
1718
PSI FILTER
1720
PSI TABLE
1722
DESCRAM -BLER
1712
KEY TABLE
1714
INPUT BUFFER
1710
PARSER
1706a
PARSER
1706b
PARSER
1706c
PID TABLE
1708
REGISTERS
1700
SYNC
1702a
SYNC
1702b
SYNC
1702c
IN BAND 1 (IB 1)
IN BAND 2 (IB 2)
OUT OF BAND (OOB)
PCR RECOVERY
1728
PCRDAC
1736
PARSED TS
1738
CLOCKS
1740
HIGH SPEED I/F
1730
CHANNEL 1
CHANNEL 2
1742
1744
BUFFER
1732
BUFFER
1734
1st AUDIO HOLD
1746
2nd AUDIO HOLD
1748
1754
1756
1758

FIG. 42

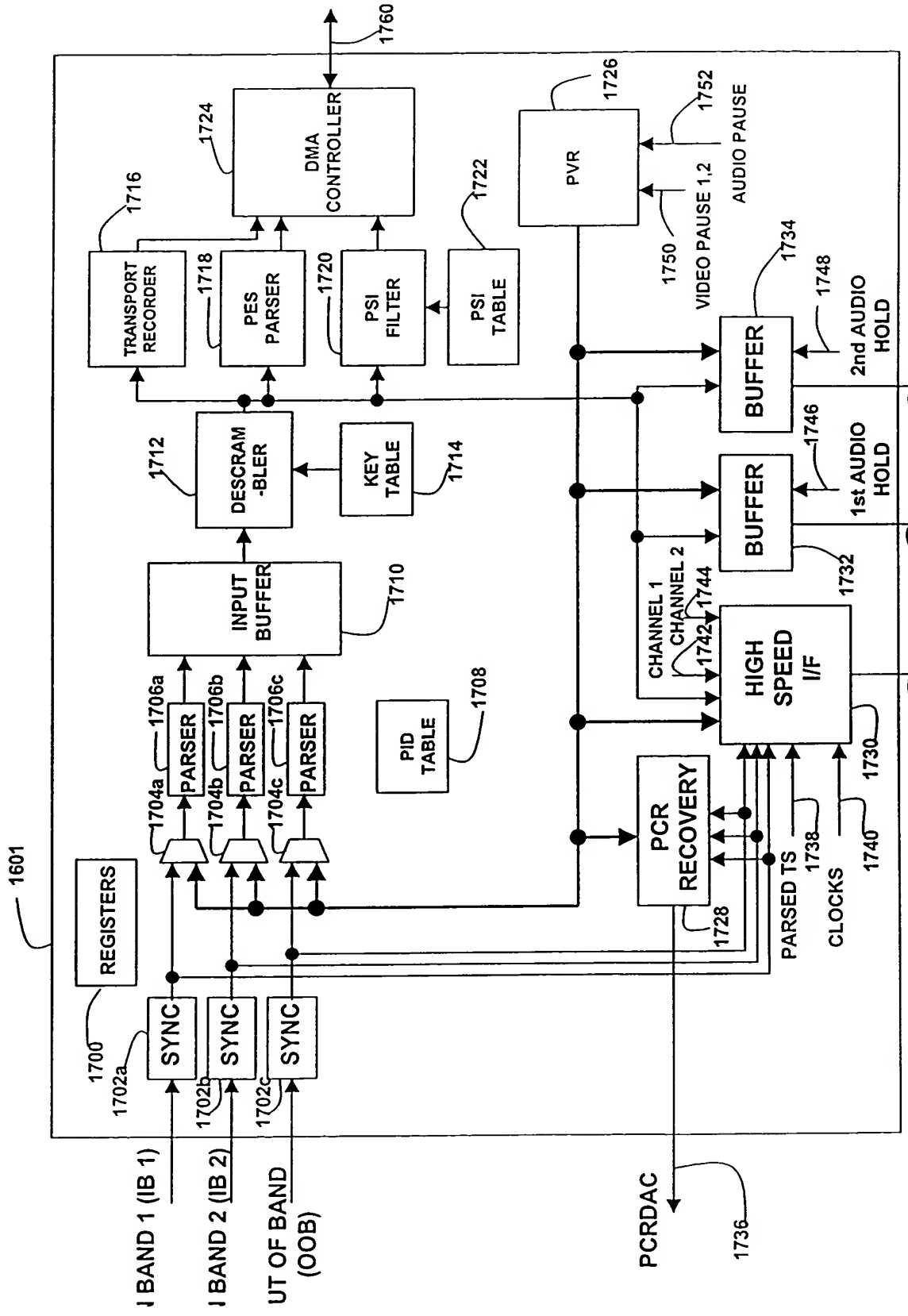
1601
REGISTERS
1700
SYNC
1702a
SYNC
1702b
SYNC
1702c
I BAND 1 (IB 1)
I BAND 2 (IB 2)
UT OF BAND (OOB)
PARSER
1704a
1706a
PARSER
1704b
1706b
PARSER
1704c
1706c
INPUT BUFFER
1710
DESCRAM -BLER
1712
KEY TABLE
1714
PID TABLE
1708
TRANSPORT RECORDER
1716
PES PARSER
1718
PSI FILTER
1720
PSI TABLE
1722
DMA CONTROLLER
1724
1760
PVR
1726
1728
PCR RECOVERY
PCRDAC
1736
1738
PARSED TS
1740
CLOCKS
1730
HIGH SPEED I/F
1732
1742
CHANNEL 1
1744
CHANNEL 2
BUFFER
1734
2nd AUDIO HOLD
1748
BUFFER
1746
1st AUDIO HOLD
1750
VIDEO PAUSE 1,2
1752
AUDIO PAUSE
1754
1756
1758

FIG. 43

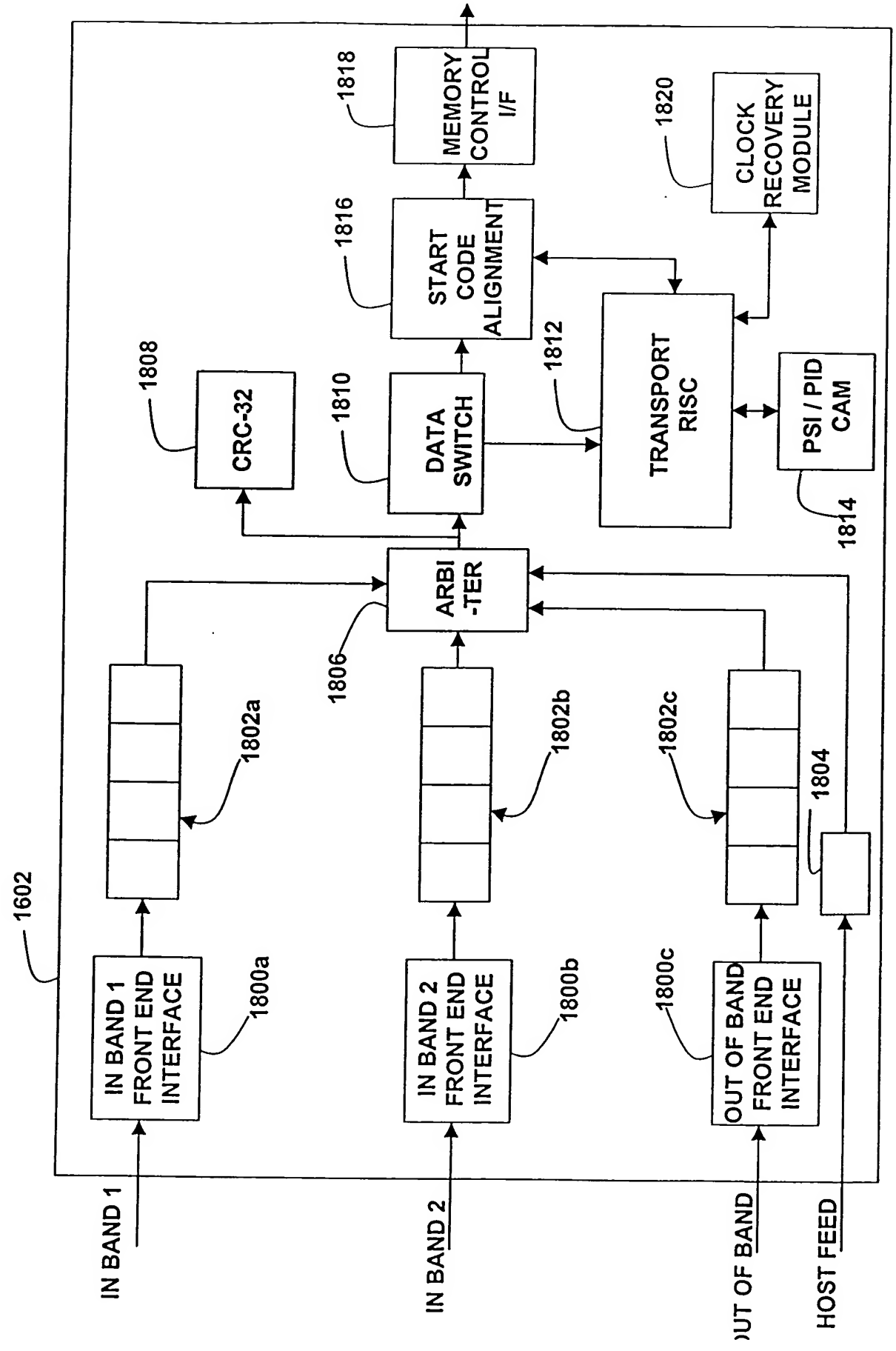
1602
IN BAND 1
IN BAND 2
OUT OF BAND
HOST FEED
IN BAND 1 FRONT END INTERFACE
1800a
IN BAND 2 FRONT END INTERFACE
1800b
OUT OF BAND FRONT END INTERFACE
1800c
1802a
1802b
1802c
1804
1806
ARBI -TER
CRC-32
1808
DATA SWITCH
1810
TRANSPORT RISC
1812
PSI / PID CAM
1814
START CODE ALIGNMENT
1816
MEMORY CONTROL I/F
1818
CLOCK RECOVERY MODULE
1820

FIG. 44

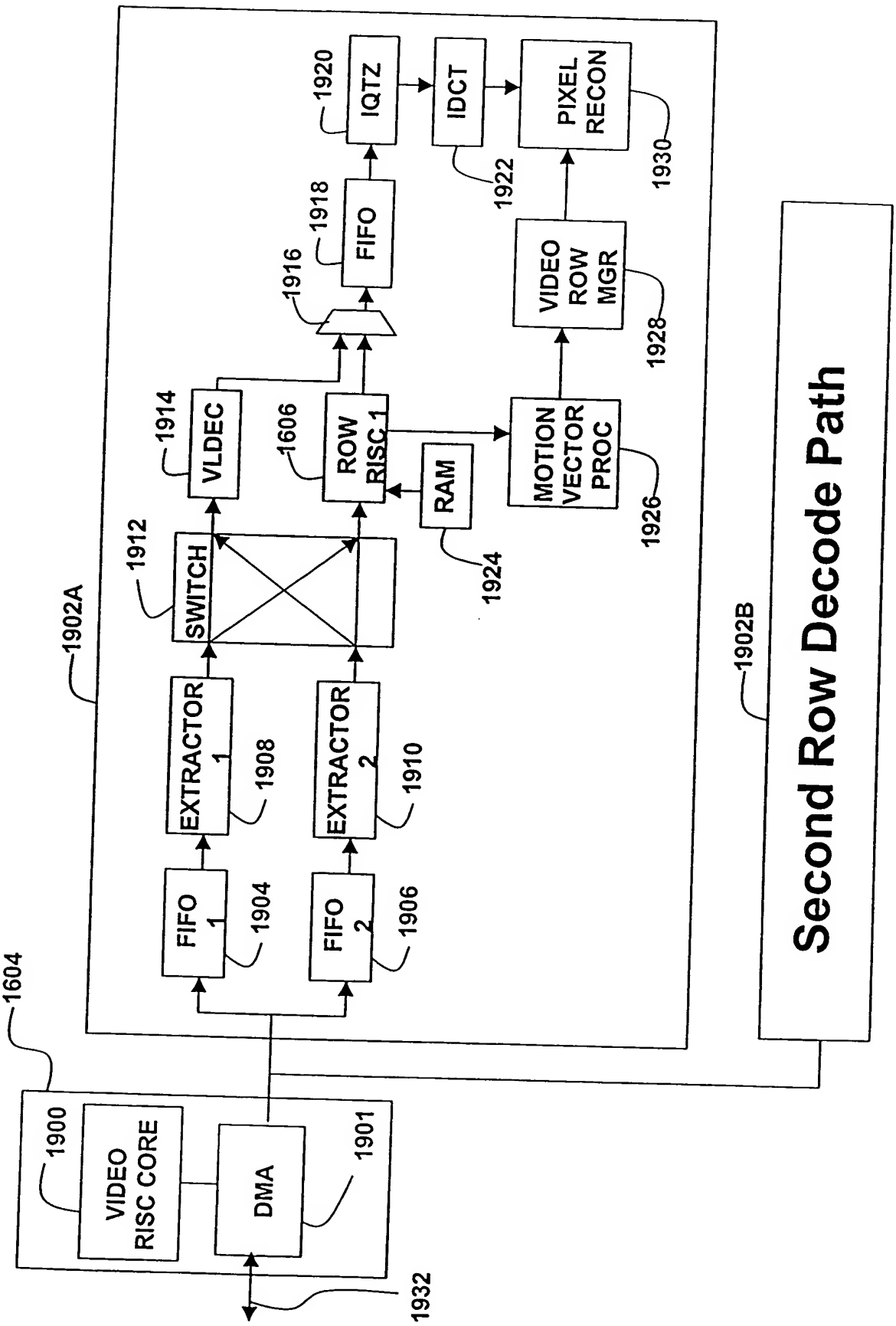
1604
1900
VIDEO RISC CORE
DMA
1901
1932
1902A
1902B
Second Row Decode Path
FIFO 1
1904
FIFO 2
1906
EXTRACTOR 1
1908
EXTRACTOR 2
1910
1912
SWITCH
1914
VLDEC
1606
ROW RISC 1
RAM
1924
1916
1918
FIFO
1920
IQTZ
IDCT
1922
PIXEL RECON
1930
MOTION VECTOR PROC
1926
VIDEO ROW MGR
1928

FIG. 45

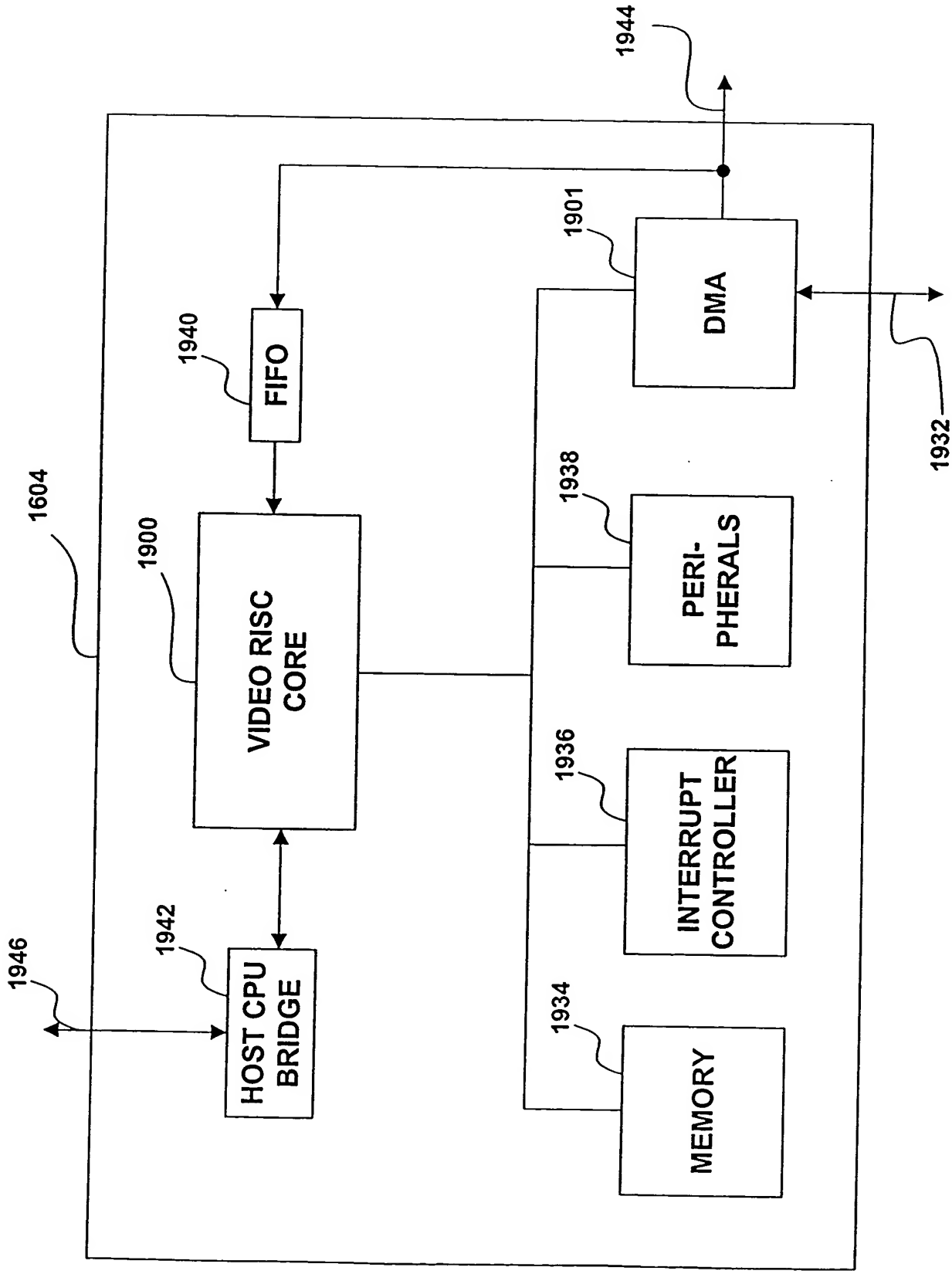
1944
1901
DMA
1940
FIFO
1604
1900
VIDEO RISC CORE
1938
PERI-PHERALS
1932
1936
INTERRUPT CONTROLLER
1942
HOST CPU BRIDGE
1946
1934
MEMORY

FIG. 46

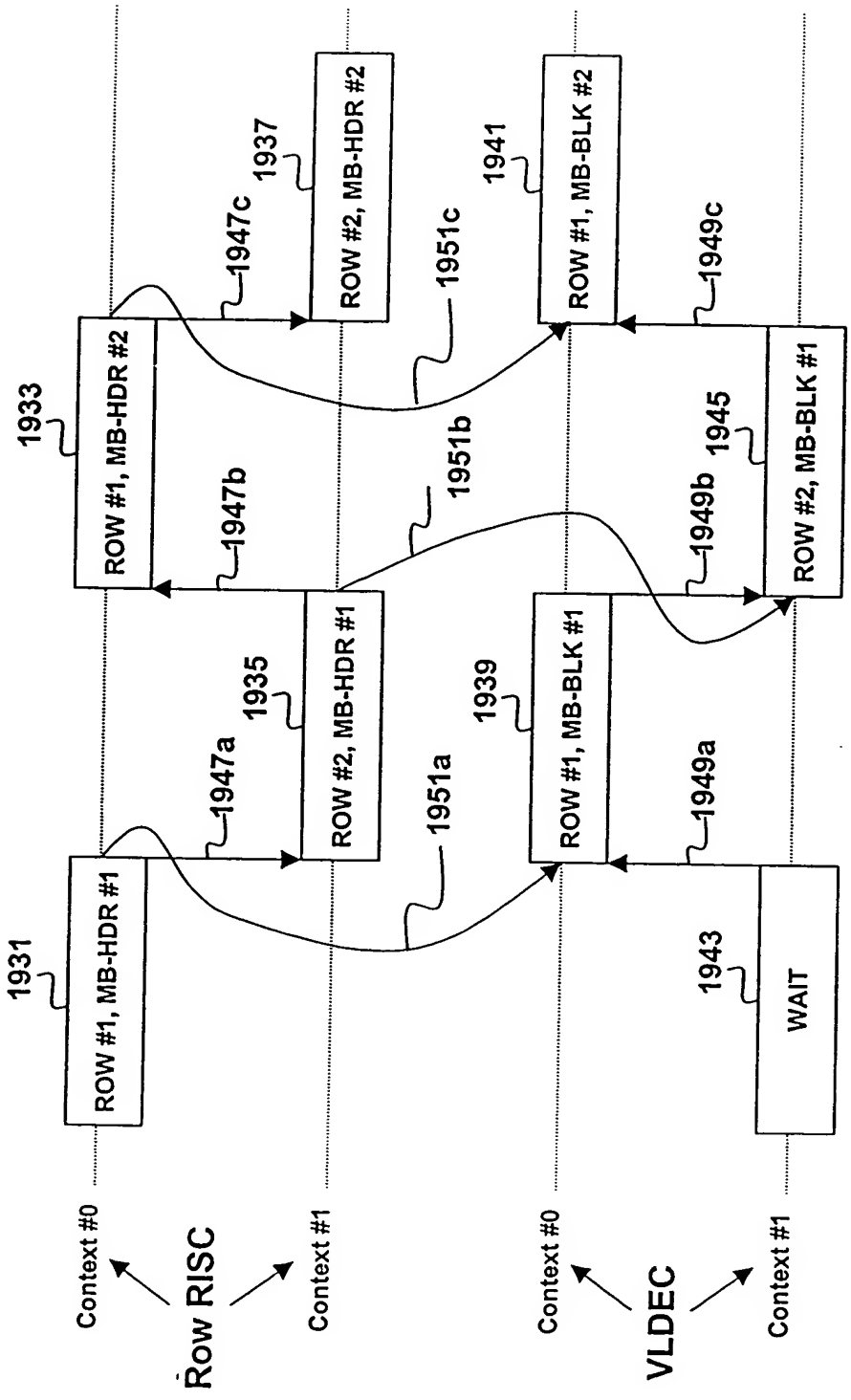
ROW #1, MB-HDR #1
1931
ROW #1, MB-HDR #2
1933
ROW #2, MB-HDR #1
1935
ROW #2, MB-HDR #2
1937
ROW #1, MB-BLK #1
1939
ROW #1, MB-BLK #2
1941
ROW #2, MB-BLK #1
1945
WAIT
1943
1947a
1947b
1947c
1949a
1949b
1949c
1951a
1951b
1951c
Context #0
Context #1
Context #0
Context #1
ROW RISC
VLDEC

FIG. 47

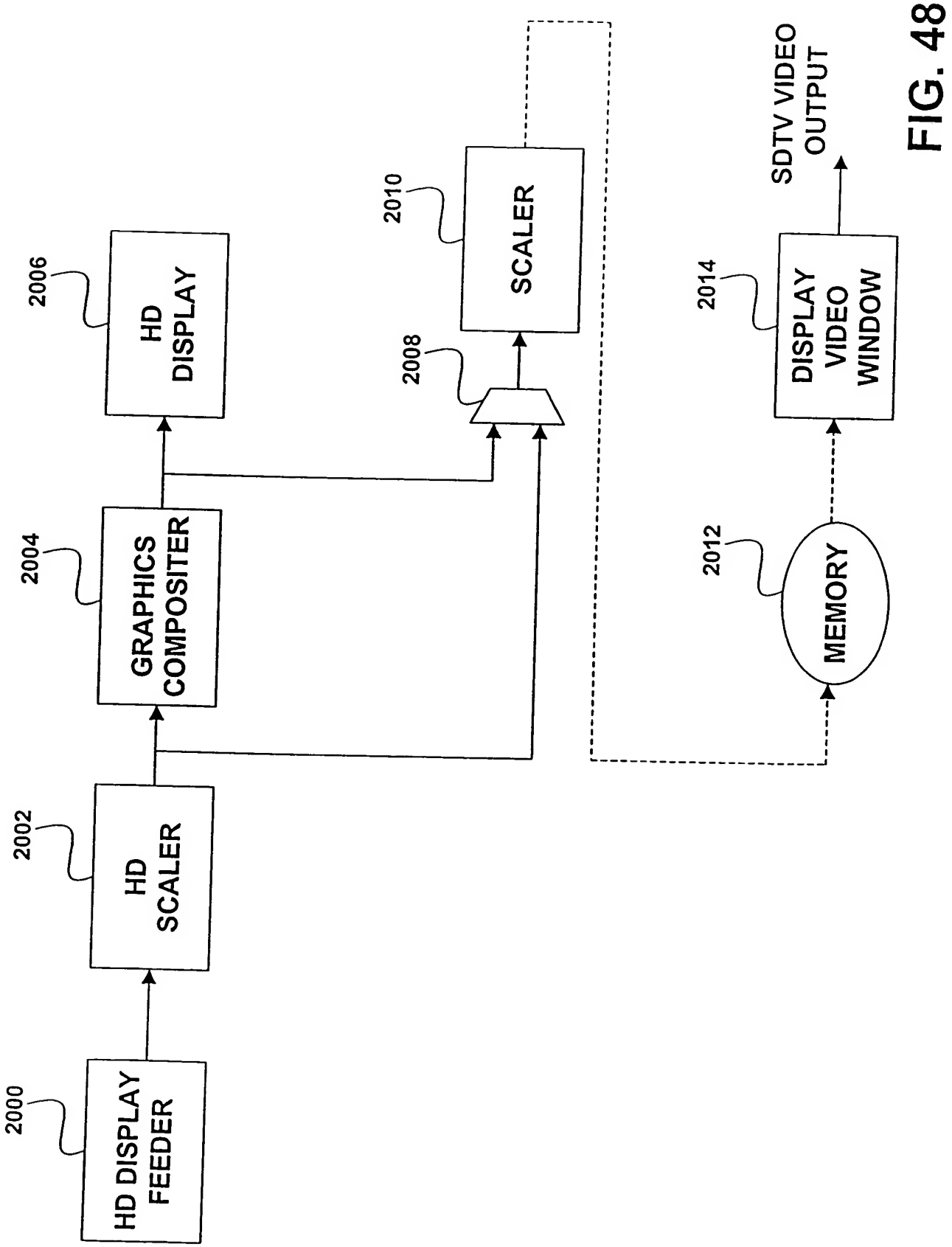
2000
HD DISPLAY FEEDER
2002
HD SCALER
2004
GRAPHICS COMPOSITER
2006
HD DISPLAY
2008
2010
SCALER
2012
MEMORY
2014
DISPLAY VIDEO WINDOW
SDTV VIDEO OUTPUT

FIG. 48

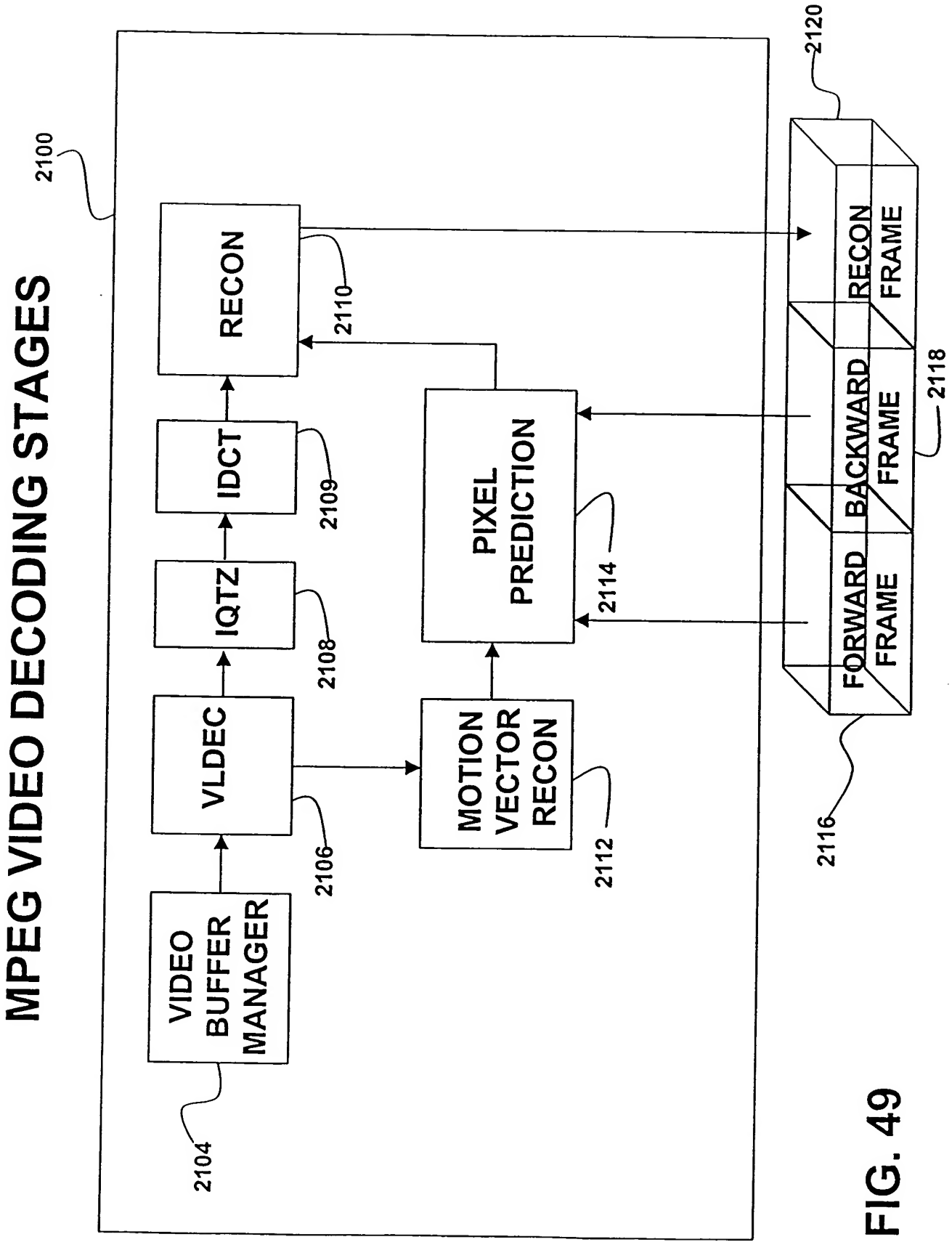
MPEG VIDEO DECODING STAGES
2100
VIDEO BUFFER MANAGER
2104
VLDEC
2106
IQTZ
2108
IDCT
2109
RECON
2110
MOTION VECTOR RECON
2112
PIXEL PREDICTION
2114
2116
2118
2120
FORWARD FRAME
BACKWARD FRAME
RECON FRAME

FIG. 49

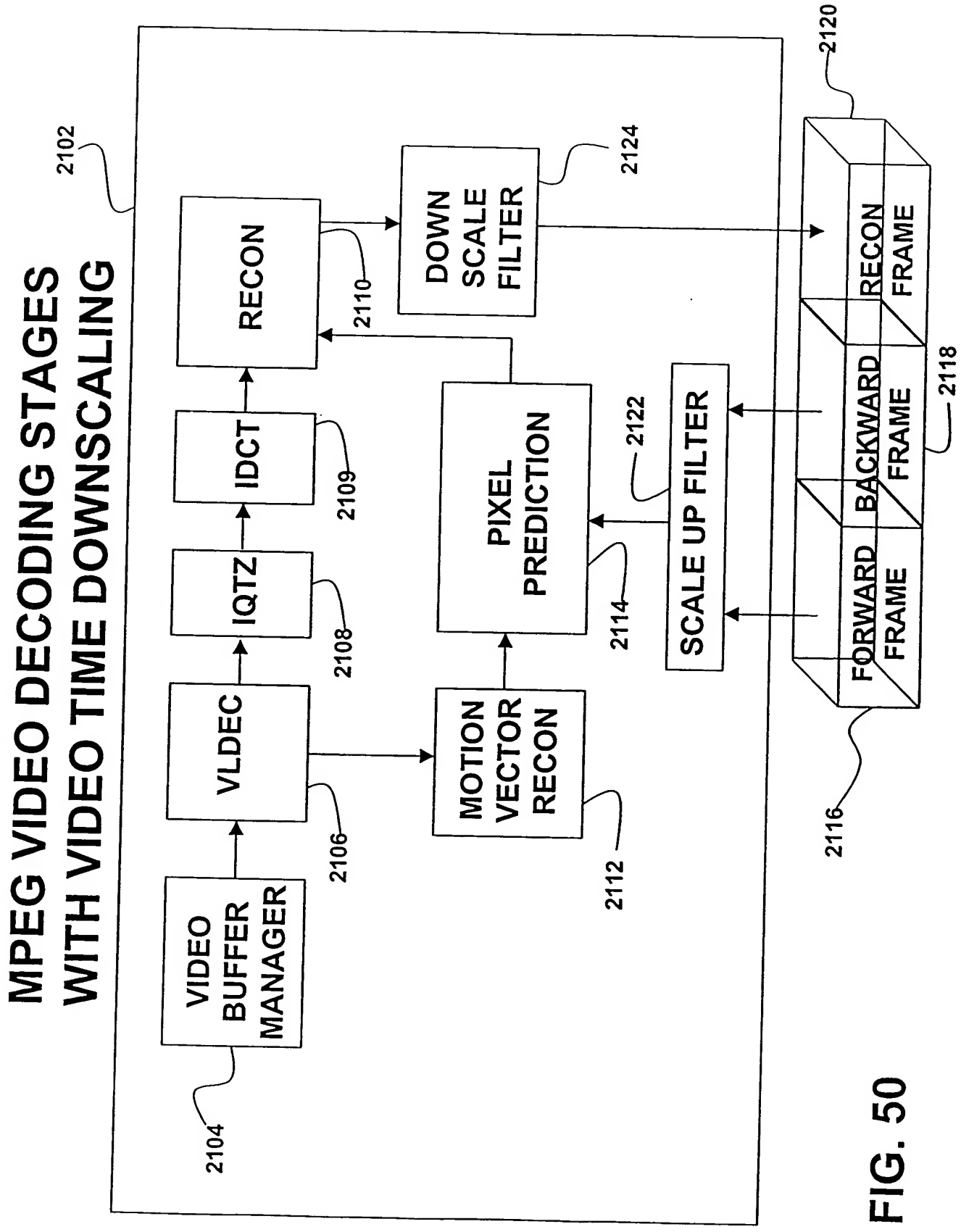
MPEG VIDEO DECODING STAGES
WITH VIDEO TIME DOWNSCALING
2102
VIDEO BUFFER MANAGER
2104
VLDEC
2106
IQTZ
2108
IDCT
2109
RECON
2110
DOWN SCALE FILTER
2124
MOTION VECTOR RECON
2112
PIXEL PREDICTION
2114
SCALE UP FILTER
2122
2120
RECON FRAME
BACKWARD FRAME
FORWARD FRAME
2118
2116

FIG. 50

FRAME-PREDICTION FOR I-PICTURES AND P-PICTURES

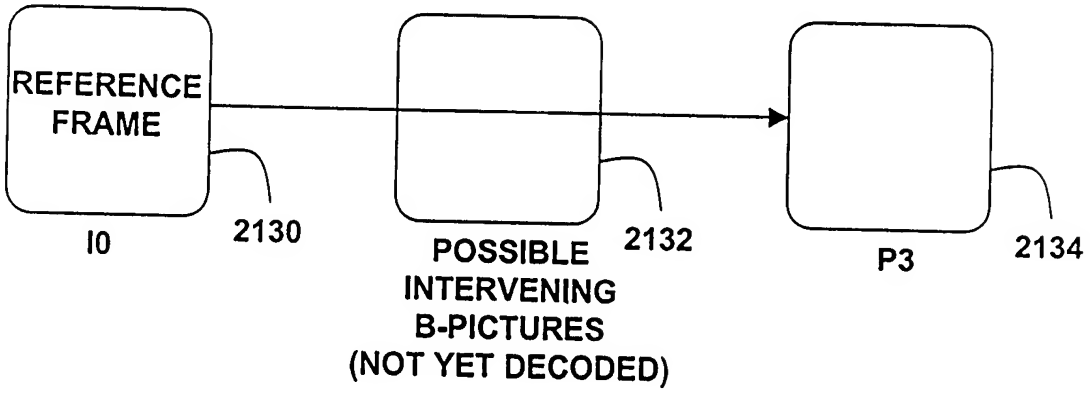

FIG. 51

FIELD PREDICTION IN A FRAME-PICTURE

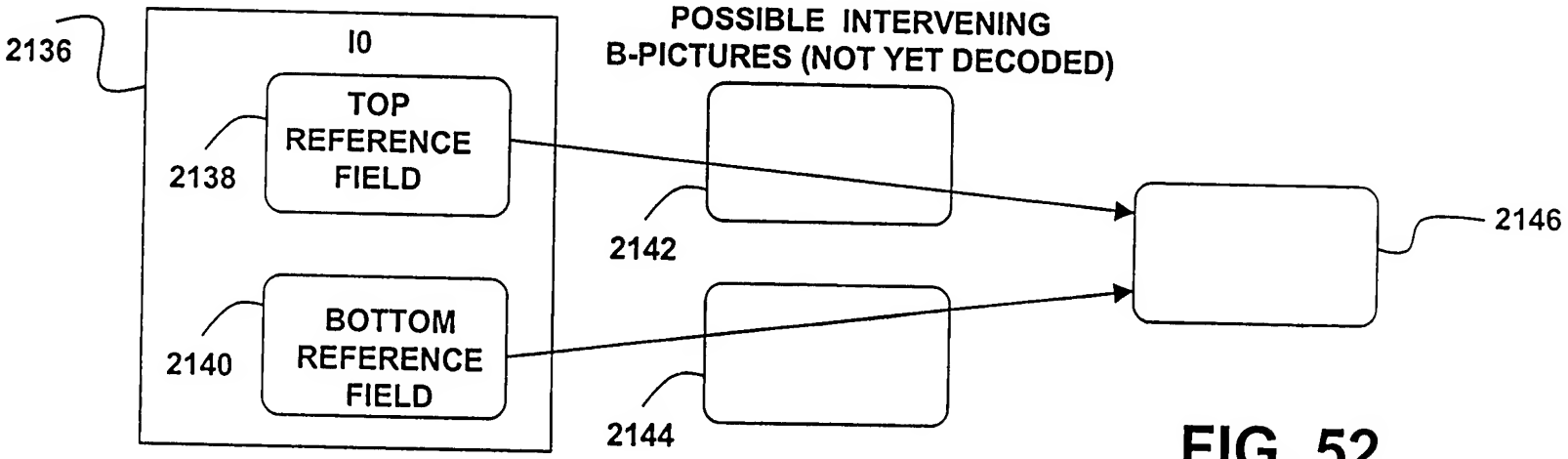

FIG. 52

Attorney: Jun-Young E. Jeon
Docket No.: 50689/JEJ/B600
Inventor(s): Ramanujan K. Valmiki, et al.
Title: Video and Graphics System with an MPEG Video Decoder for Concurrent Multi-Row Decoding
Sheet 51 of 70

PREDICTION OF THE FIRST FIELD-PICTURE

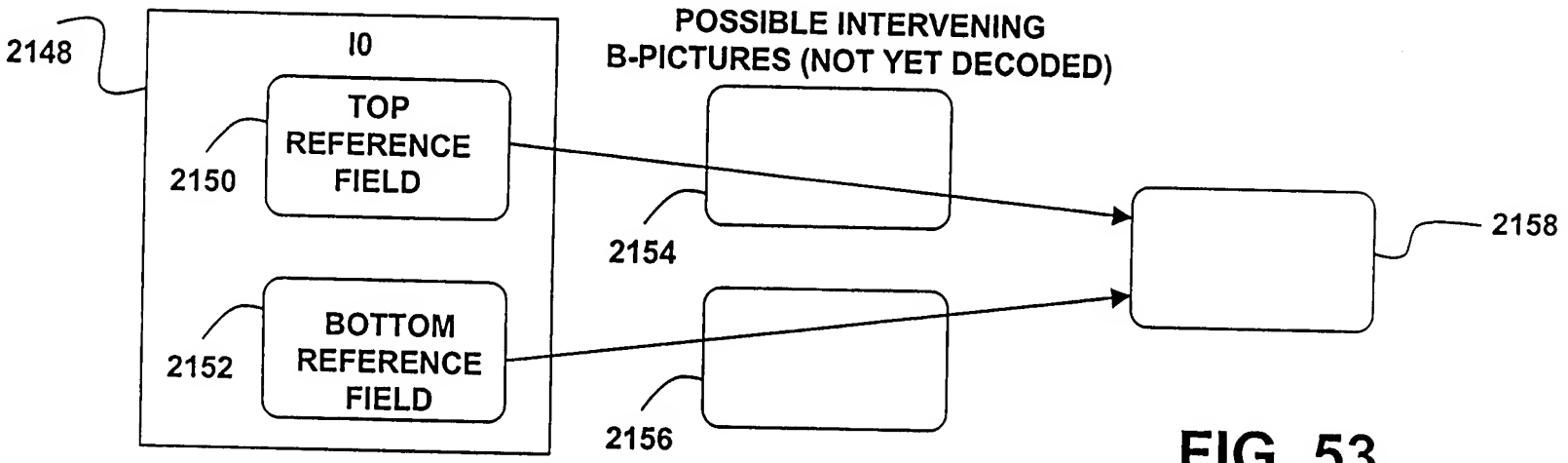

FIG. 53

PREDICTION OF THE "BOTTOM FIELD" SECOND FIELD-PICTURE

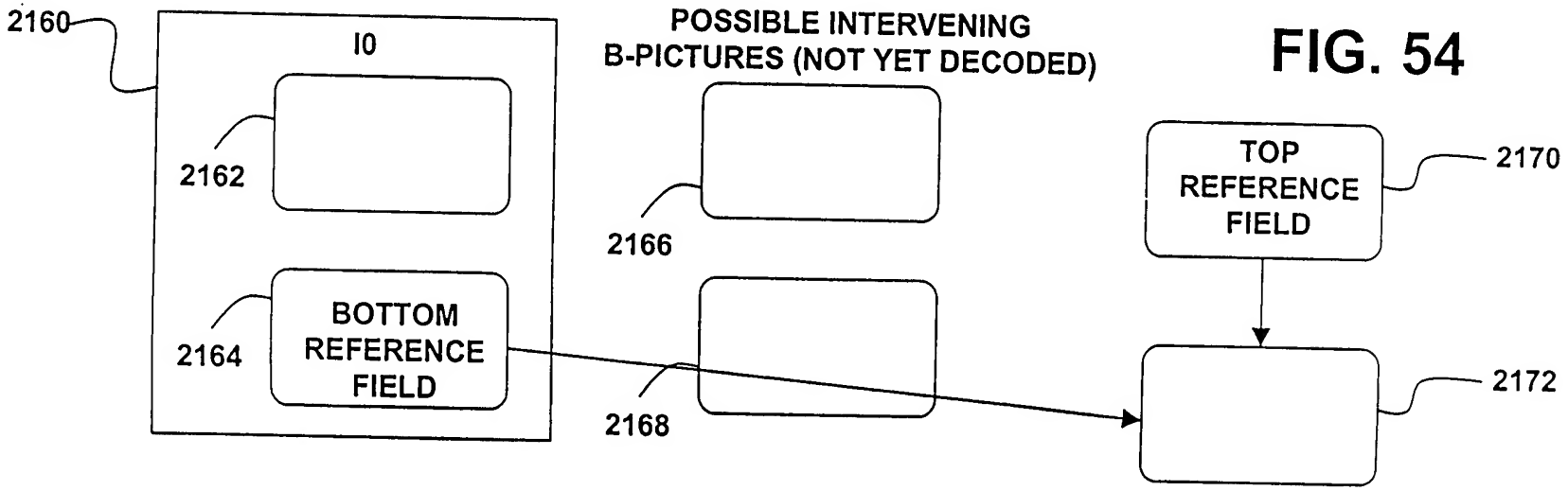

FIG. 54

Attorney: Jun-Young E. Jeon
Docket No.: 50689/JEJ/B600
Inventor(s): Ramanujan K. Valmiki, et al.
Title: Video and Graphics System with an MPEG Video Decoder for Concurrent Multi-Row Decoding
Sheet 52 of 70

PREDICTION OF THE "TOP FIELD" SECOND FIELD-PICTURE

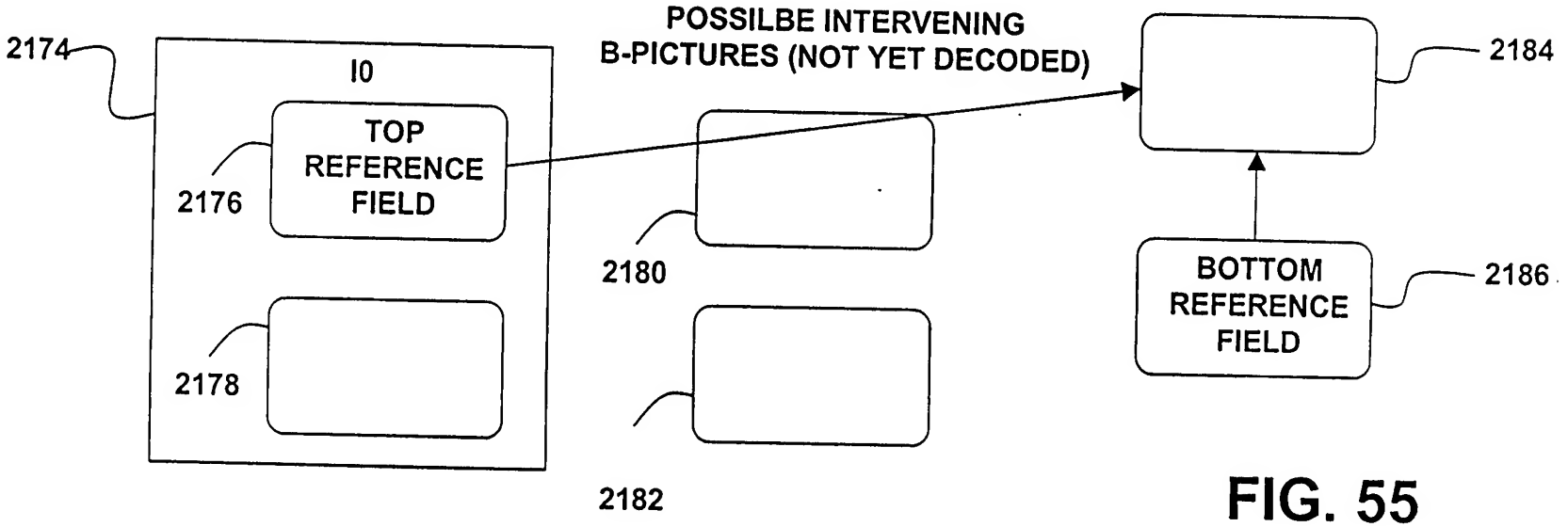

FIG. 55

FIELD-PREDICTIONOF B FIELD PICTURES OR B FRAME PICTURES

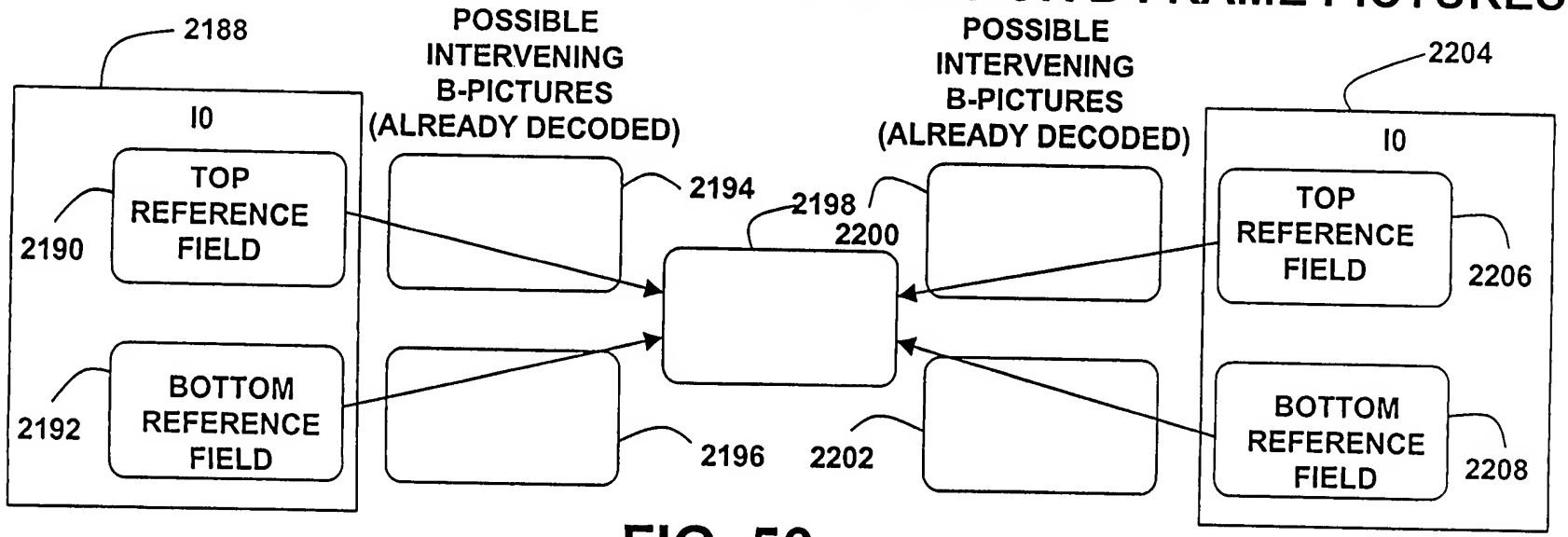

FIG. 56

Attorney: Jun-Young E. Jeon
Docket No.: 50689/JEJ/B600
Inventor(s): Ramanujan K. Valmiki, et al.
Title: Video and Graphics System with an MPEG Video Decoder for Concurrent Multi-Row Decoding
Sheet 53 of 70

FRAME-PREDICTIONS FOR B-PICTURES

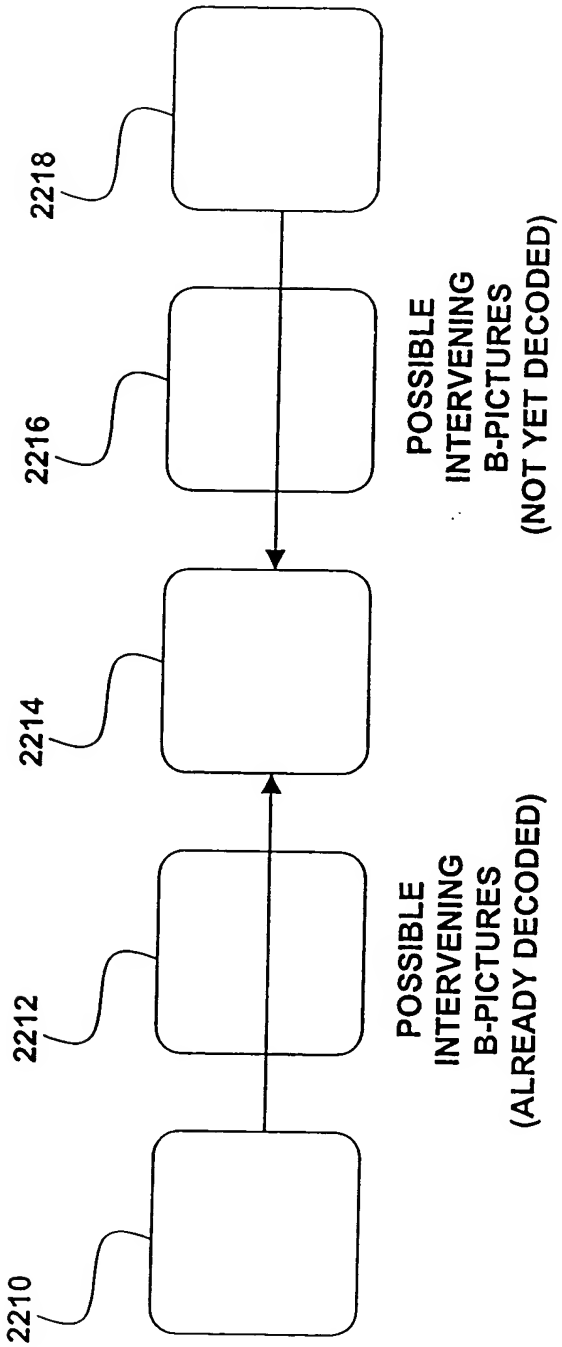

FIG. 57

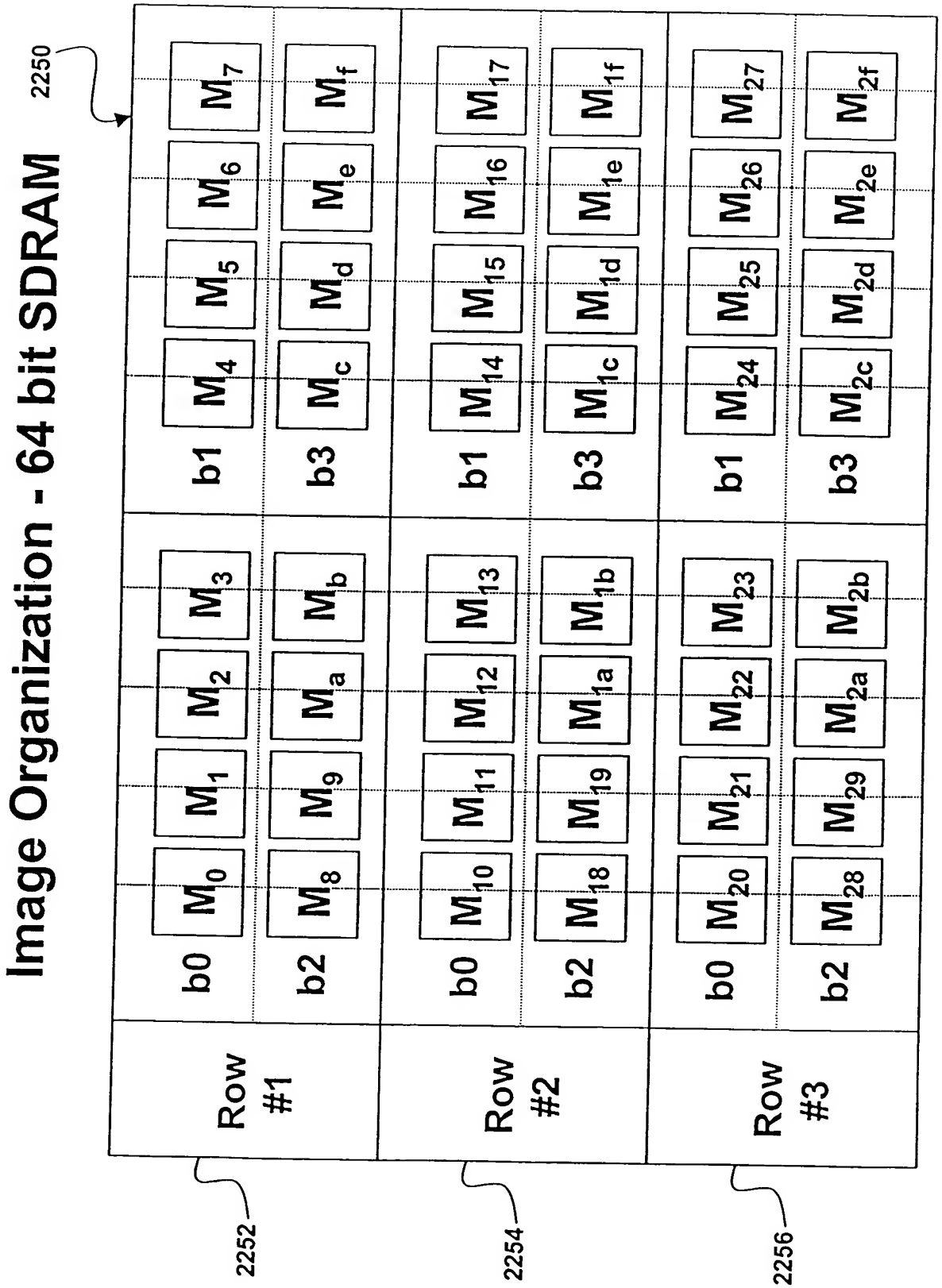
Image Organization - 64 bit SDRAM
2250
Row #1
Row #2
Row #3
2252
2254
2256
b0
b1
b2
b3
M0 M1 M2 M3 M4 M5 M6 M7
M8 M9 Ma Mb Mc Md Me Mf
M10 M11 M12 M13 M14 M15 M16 M17
M18 M19 M1a M1b M1c M1d M1e M1f
M20 M21 M22 M23 M24 M25 M26 M27
M28 M29 M2a M2b M2c M2d M2e M2f

FIG. 58

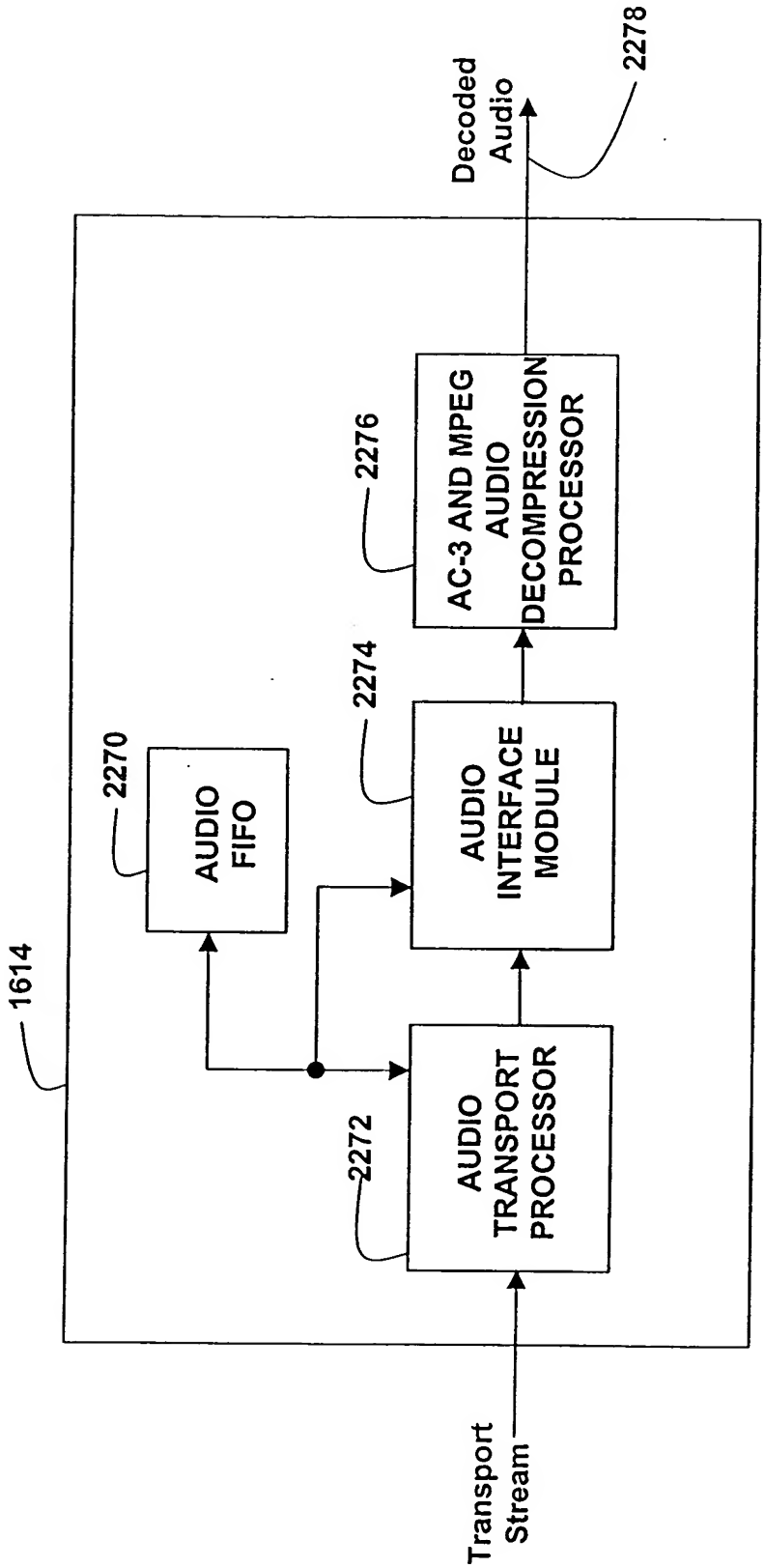
Transport Stream
1614
AUDIO TRANSPORT PROCESSOR
2272
AUDIO INTERFACE MODULE
2274
AUDIO FIFO
2270
AC-3 AND MPEG AUDIO DECOMPRESSION PROCESSOR
2276
Decoded Audio
2278

FIG. 59

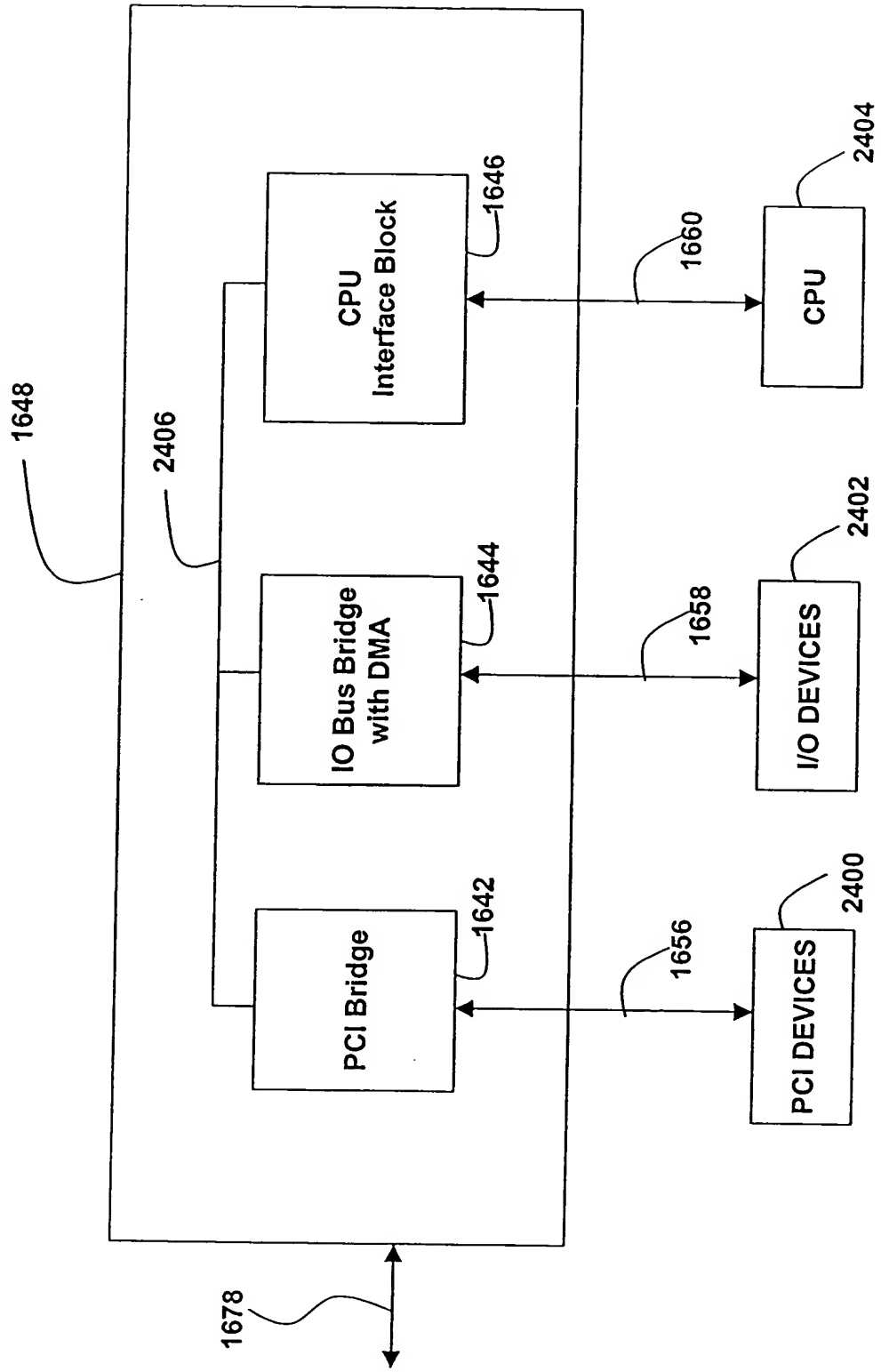
1648
2406
CPU Interface Block
1646
1660
CPU
2404
IO Bus Bridge with DMA
1644
1658
I/O DEVICES
2402
PCI Bridge
1642
1656
PCI DEVICES
2400
1678

FIG. 60

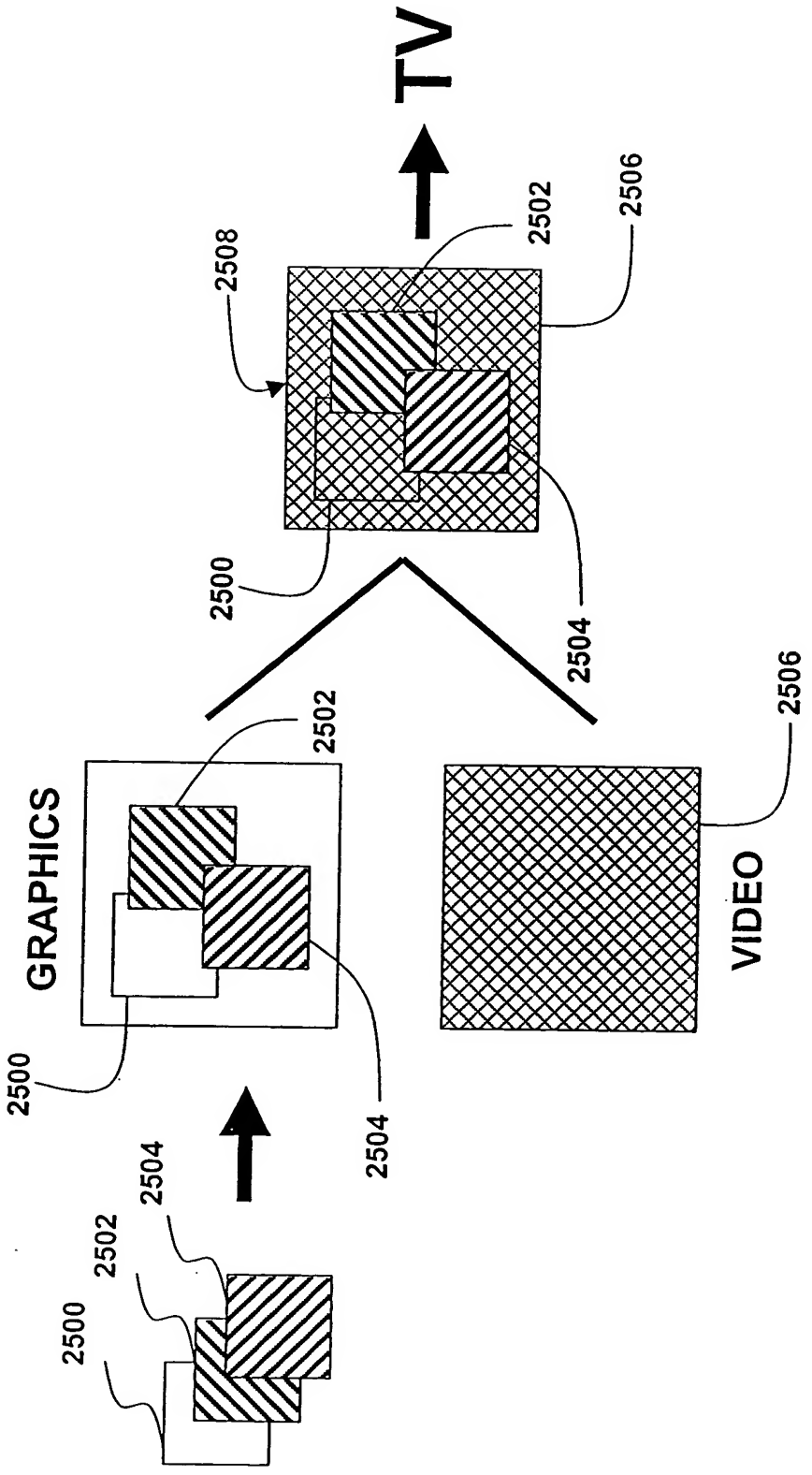
TV
2502
2506
2508
2500
2504
2502
2506
GRAPHICS
VIDEO
2500
2504
2504
2502
2500

FIG. 61

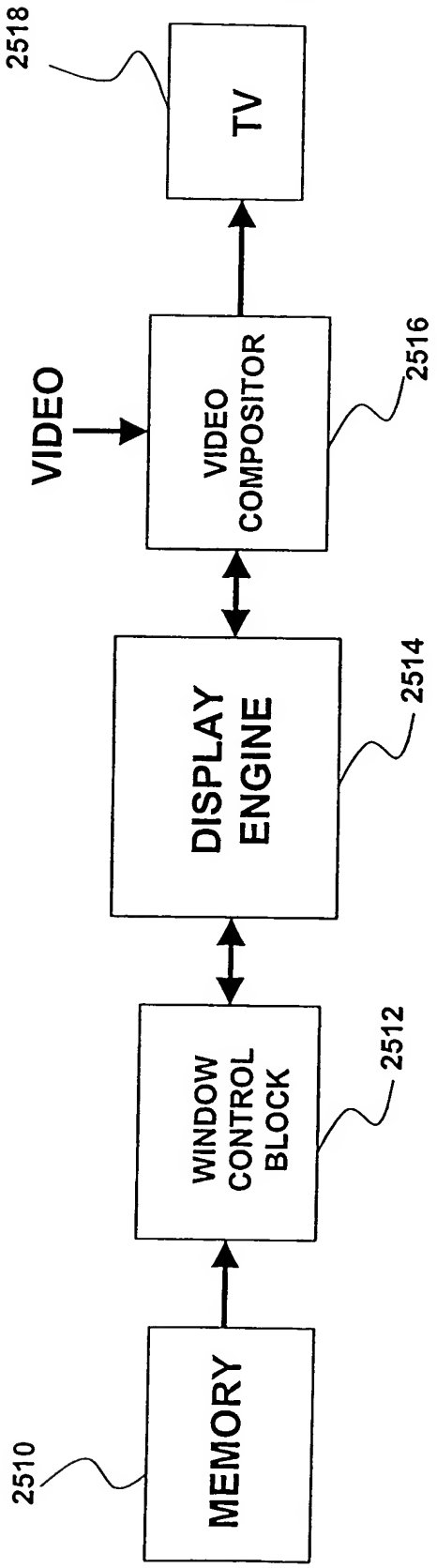
2518
TV
VIDEO
VIDEO COMPOSITOR
2516
DISPLAY ENGINE
2514
WINDOW CONTROL BLOCK
2512
MEMORY
2510

FIG. 62

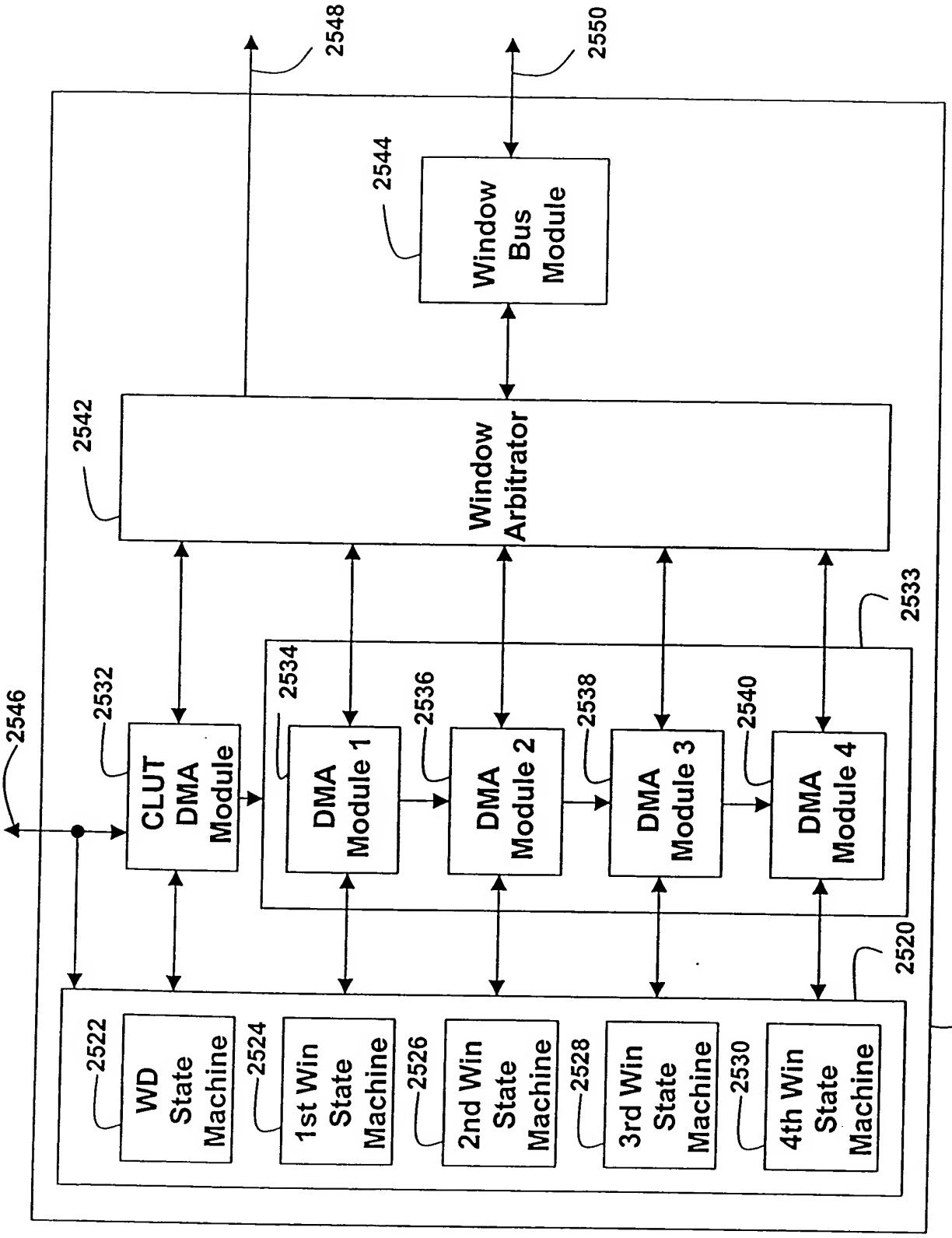
2548
2550
2544
Window Bus Module
2542
Window Arbitrator
2533
2534
2536
2538
2540
2532
2546
CLUT DMA Module
DMA Module 1
DMA Module 2
DMA Module 3
DMA Module 4
2512
2520
2522
WD State Machine
2524
1st Win State Machine
2526
2nd Win State Machine
2528
3rd Win State Machine
2530
4th Win State Machine

FIG. 63

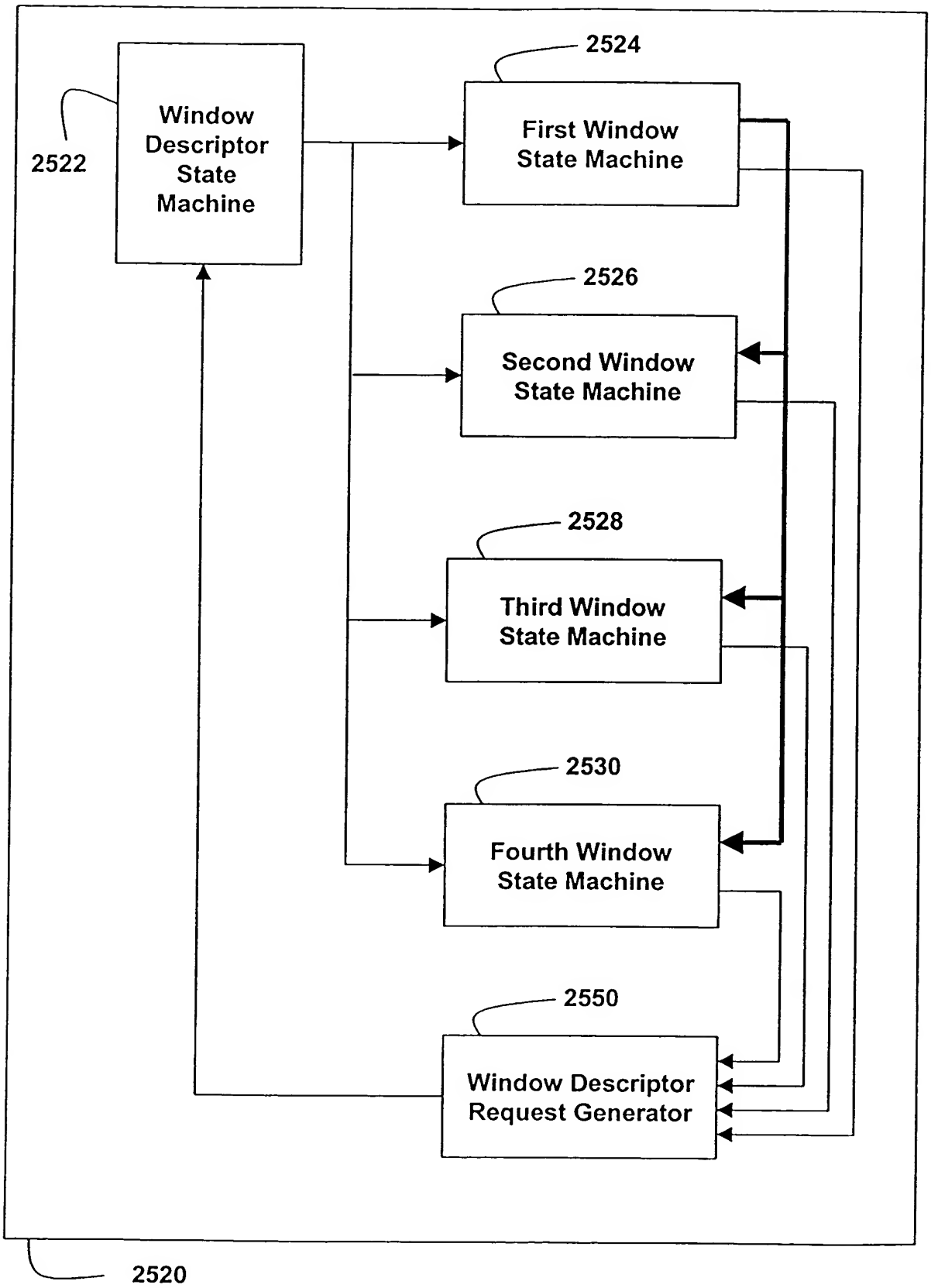
2522
Window Descriptor State Machine
2524
First Window State Machine
2526
Second Window State Machine
2528
Third Window State Machine
2530
Fourth Window State Machine
2550
Window Descriptor Request Generator
2520

FIG. 64

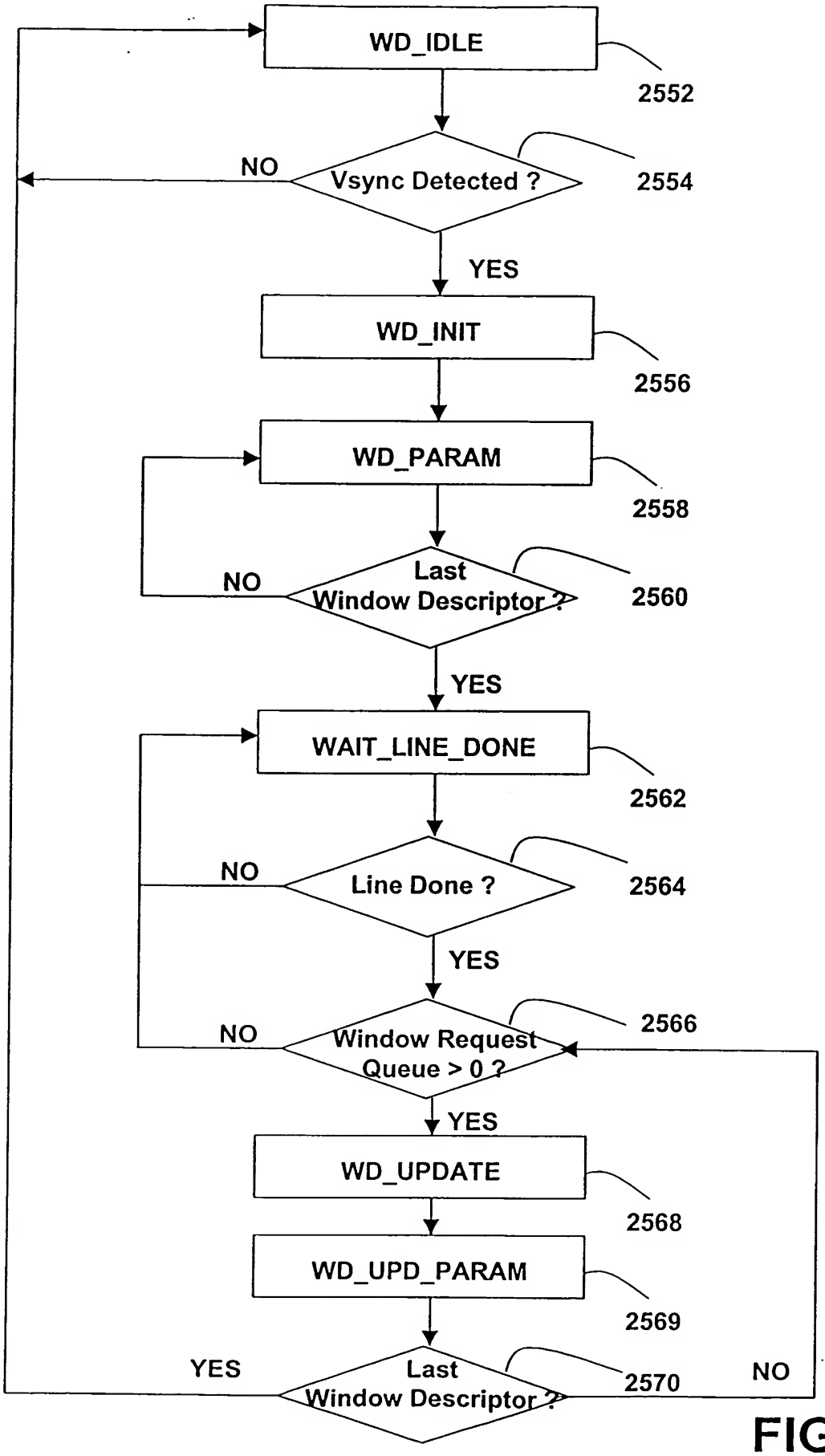
WD_IDLE
2552
Vsync Detected ?
NO
2554
YES
WD_INIT
2556
WD_PARAM
2558
Last Window Descriptor ?
NO
2560
YES
WAIT_LINE_DONE
2562
Line Done ?
NO
2564
YES
Window Request Queue > 0 ?
NO
2566
YES
WD_UPDATE
2568
WD_UPD_PARAM
2569
Last Window Descriptor ?
YES
2570
NO

FIG. 65

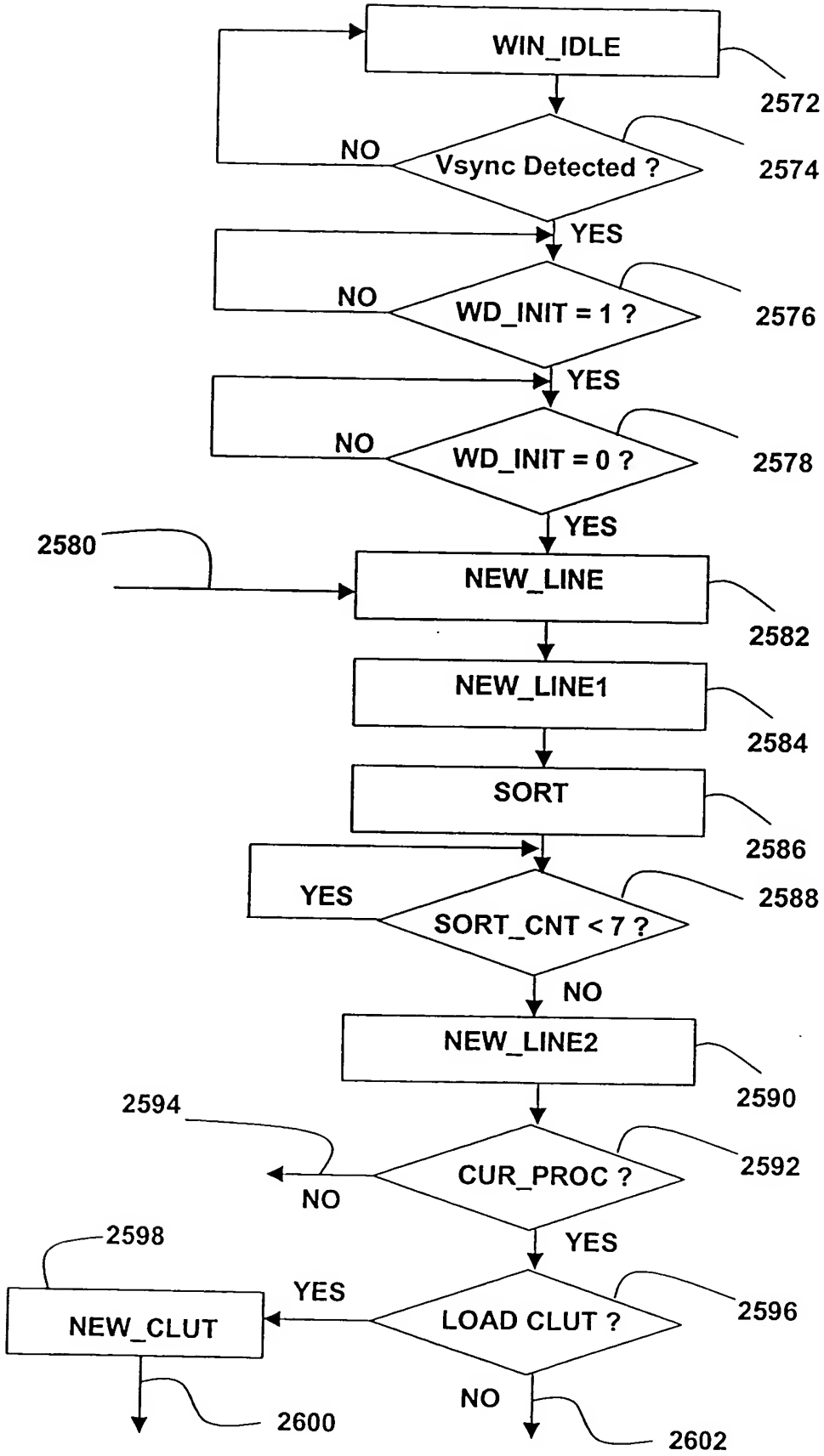
WIN_IDLE
2572
NO
Vsync Detected ?
2574
YES
NO
WD_INIT = 1 ?
2576
YES
NO
WD_INIT = 0 ?
2578
YES
2580
NEW_LINE
2582
NEW_LINE1
2584
SORT
2586
YES
SORT_CNT < 7 ?
2588
NO
NEW_LINE2
2590
2594
NO
CUR_PROC ?
2592
YES
2598
YES
NEW_CLUT
LOAD CLUT ?
2596
NO
2600
2602

FIG. 66

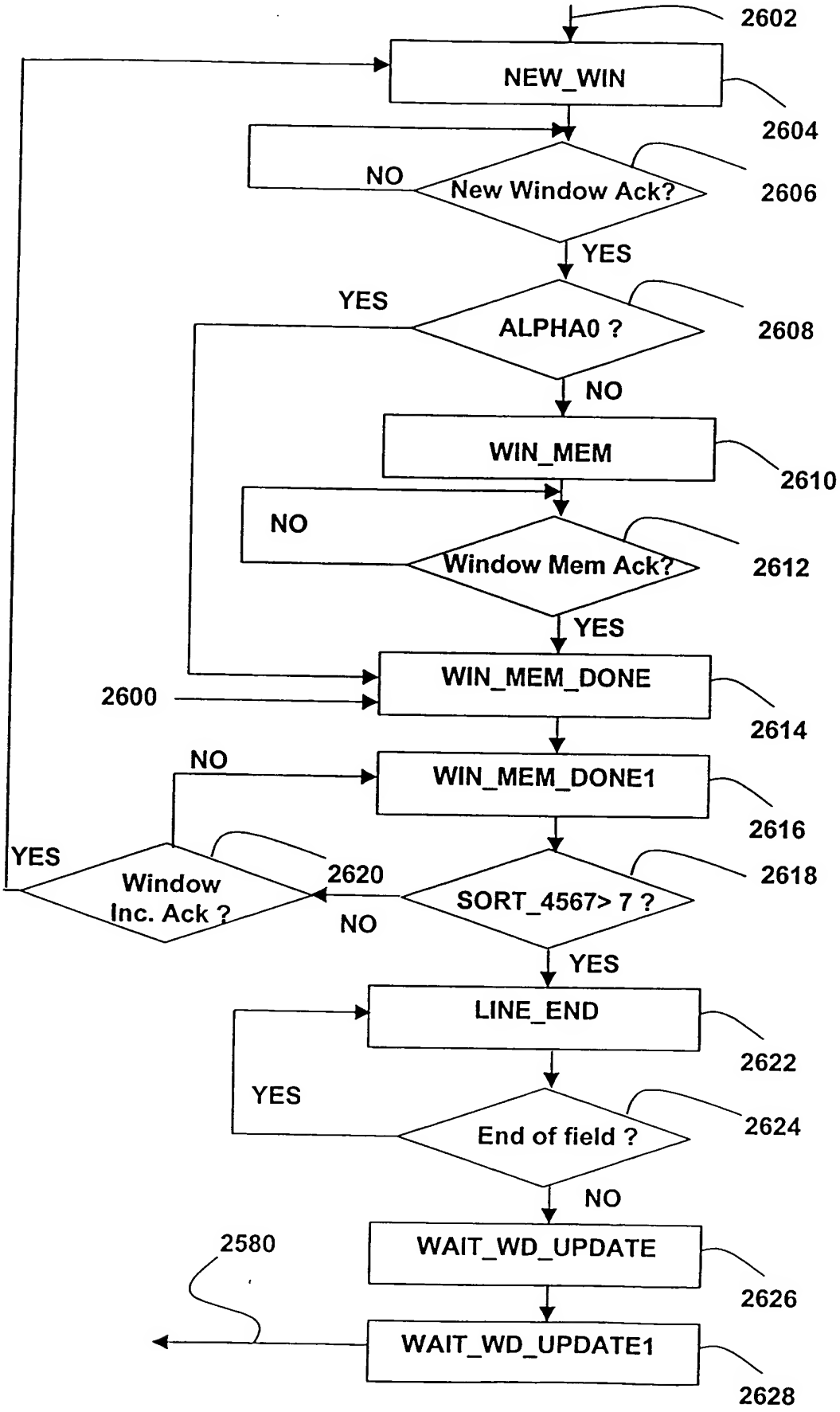
2602
NEW_WIN
2604
NO
New Window Ack?
2606
YES
YES
ALPHA0 ?
2608
NO
WIN_MEM
2610
NO
Window Mem Ack?
2612
YES
WIN_MEM_DONE
2600
2614
NO
WIN_MEM_DONE1
2616
YES
Window Inc. Ack ?
2620
SORT_4567> 7 ?
2618
NO
YES
LINE_END
2622
YES
End of field ?
2624
NO
2580
WAIT_WD_UPDATE
2626
WAIT_WD_UPDATE1
2628

FIG. 67

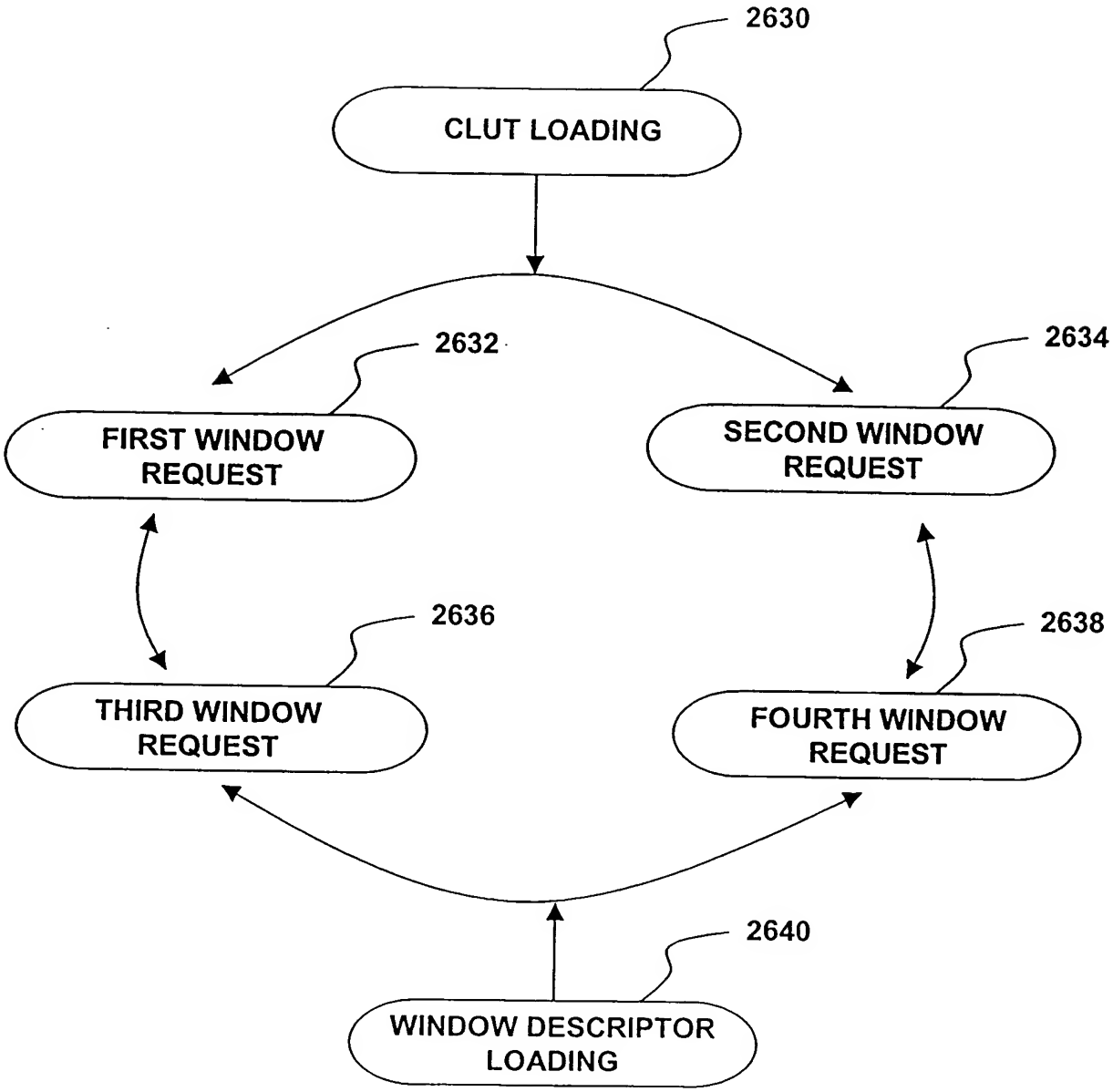
2630
CLUT LOADING
2632
FIRST WINDOW REQUEST
2634
SECOND WINDOW REQUEST
2636
THIRD WINDOW REQUEST
2638
FOURTH WINDOW REQUEST
2640
WINDOW DESCRIPTOR LOADING

FIG. 68

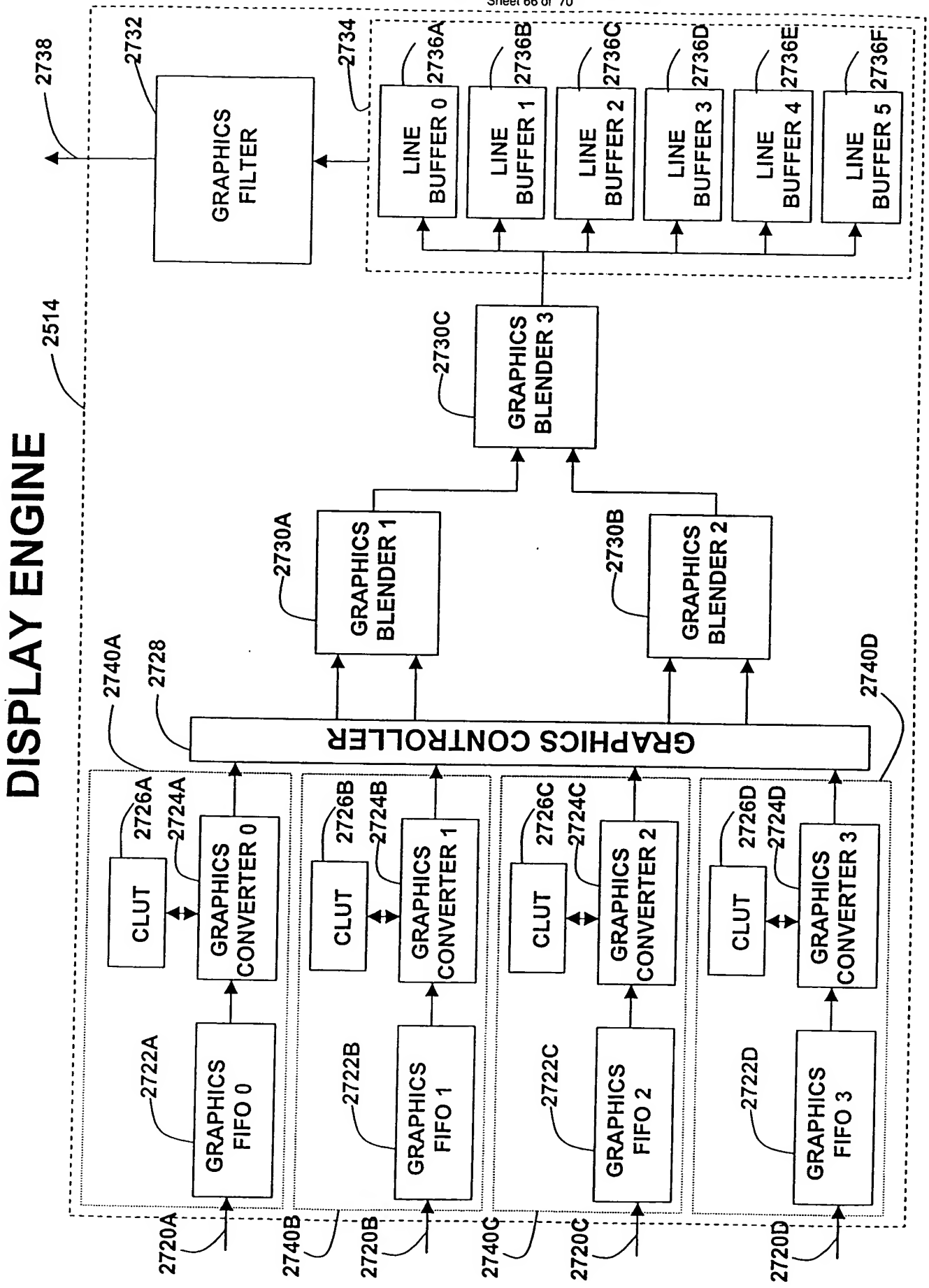
DISPLAY ENGINE
2514
2738
2732
GRAPHICS FILTER
2734
LINE BUFFER 0
LINE BUFFER 1
LINE BUFFER 2
LINE BUFFER 3
LINE BUFFER 4
LINE BUFFER 5
2736A
2736B
2736C
2736D
2736E
2736F
2730C
GRAPHICS BLENDER 3
2730A
GRAPHICS BLENDER 1
2730B
GRAPHICS BLENDER 2
2740A
2728
GRAPHICS CONTROLLER
2740D
CLUT
GRAPHICS CONVERTER 0
2726A
2724A
CLUT
GRAPHICS CONVERTER 1
2726B
2724B
CLUT
GRAPHICS CONVERTER 2
2726C
2724C
CLUT
GRAPHICS CONVERTER 3
2726D
2724D
GRAPHICS FIFO 0
2722A
GRAPHICS FIFO 1
2722B
GRAPHICS FIFO 2
2722C
GRAPHICS FIFO 3
2722D
2720A
2740B
2720B
2740C
2720C
2720D

FIG. 69

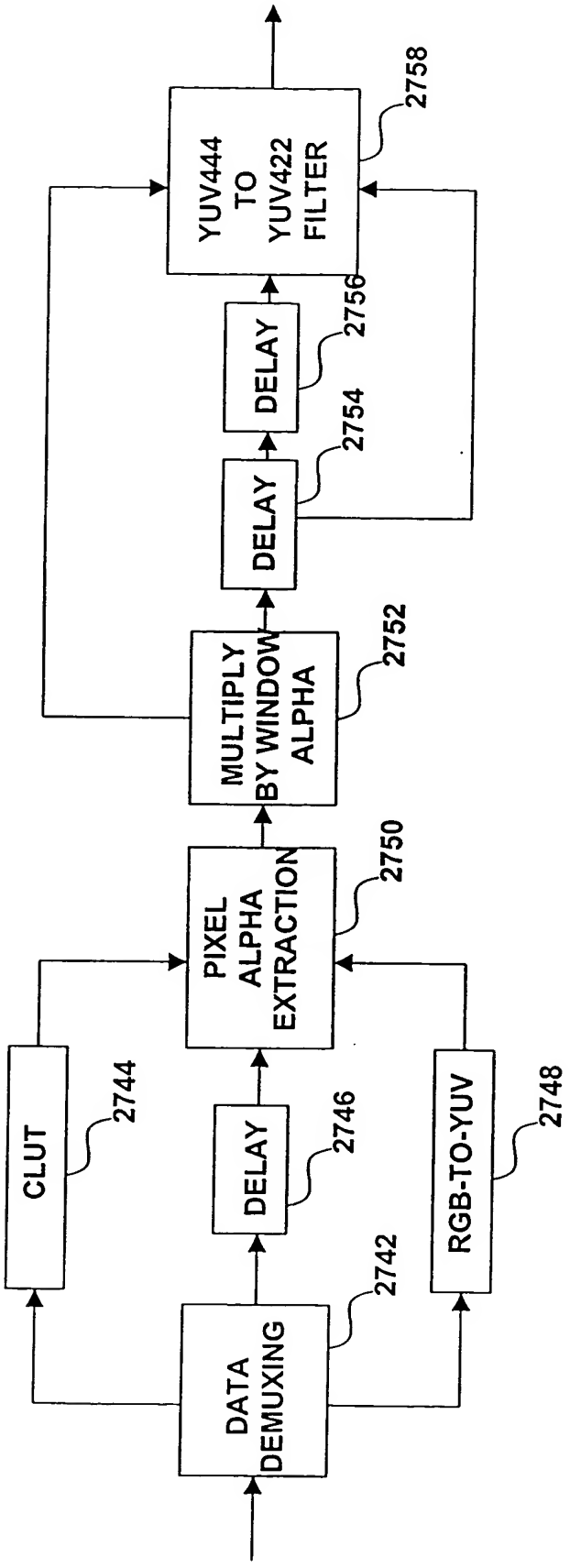
DATA DEMUXING
2742
CLUT
2744
DELAY
2746
RGB-TO-YUV
2748
PIXEL ALPHA EXTRACTION
2750
MULTIPLY BY WINDOW ALPHA
2752
DELAY
2754
DELAY
2756
YUV444 TO YUV422 FILTER
2758

FIG. 70

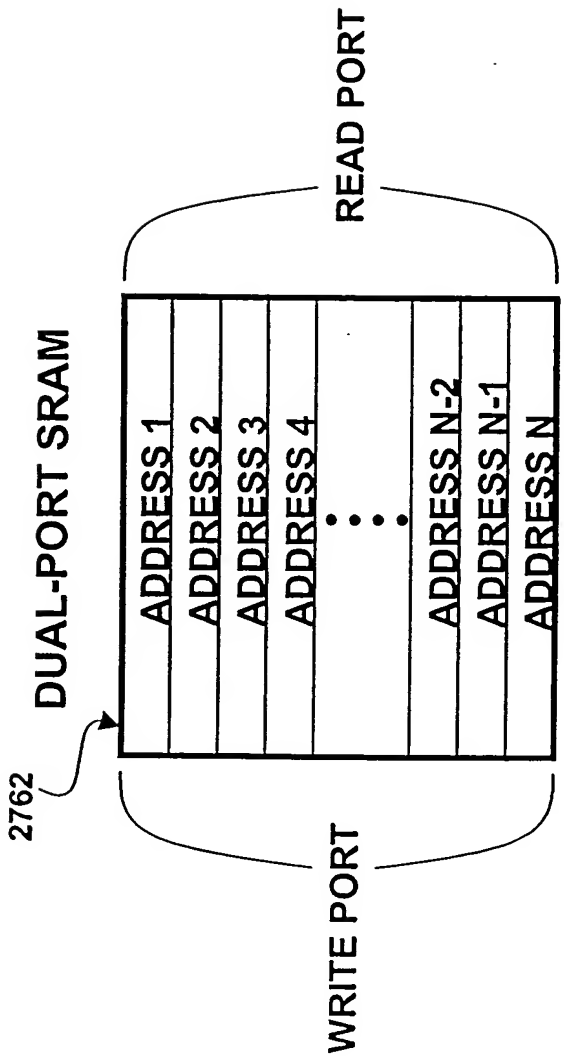
DUAL-PORT SRAM
2762
ADDRESS 1
ADDRESS 2
ADDRESS 3
ADDRESS 4
ADDRESS N-2
ADDRESS N-1
ADDRESS N
READ PORT
WRITE PORT

FIG. 71

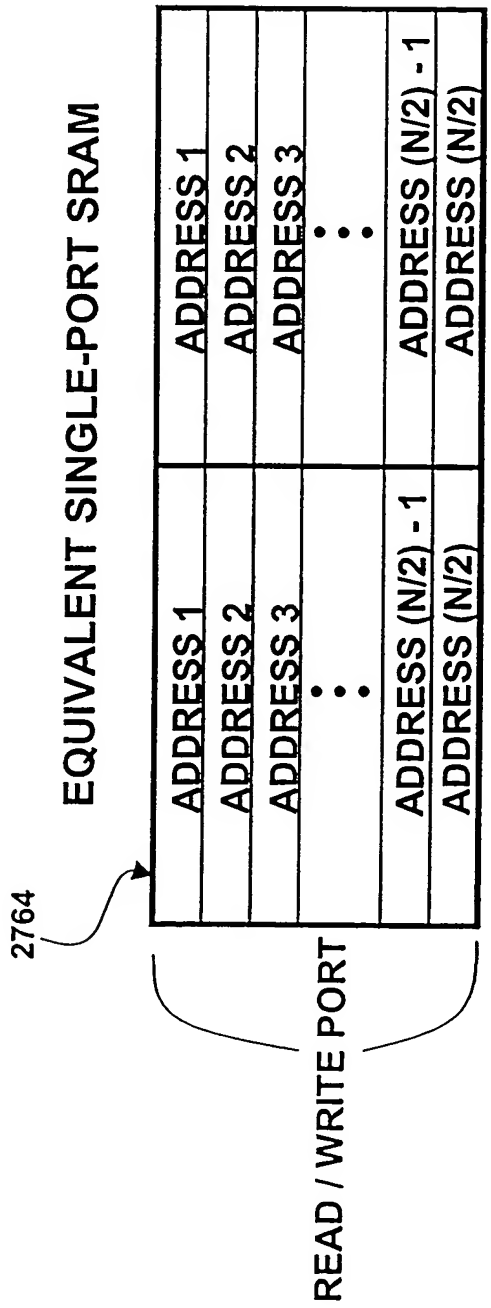
EQUIVALENT SINGLE-PORT SRAM
2764
ADDRESS 1
ADDRESS 2
ADDRESS 3
ADDRESS (N/2) - 1
ADDRESS (N/2)
ADDRESS 1
ADDRESS 2
ADDRESS 3
ADDRESS (N/2) - 1
ADDRESS (N/2)
READ / WRITE PORT

FIG. 72

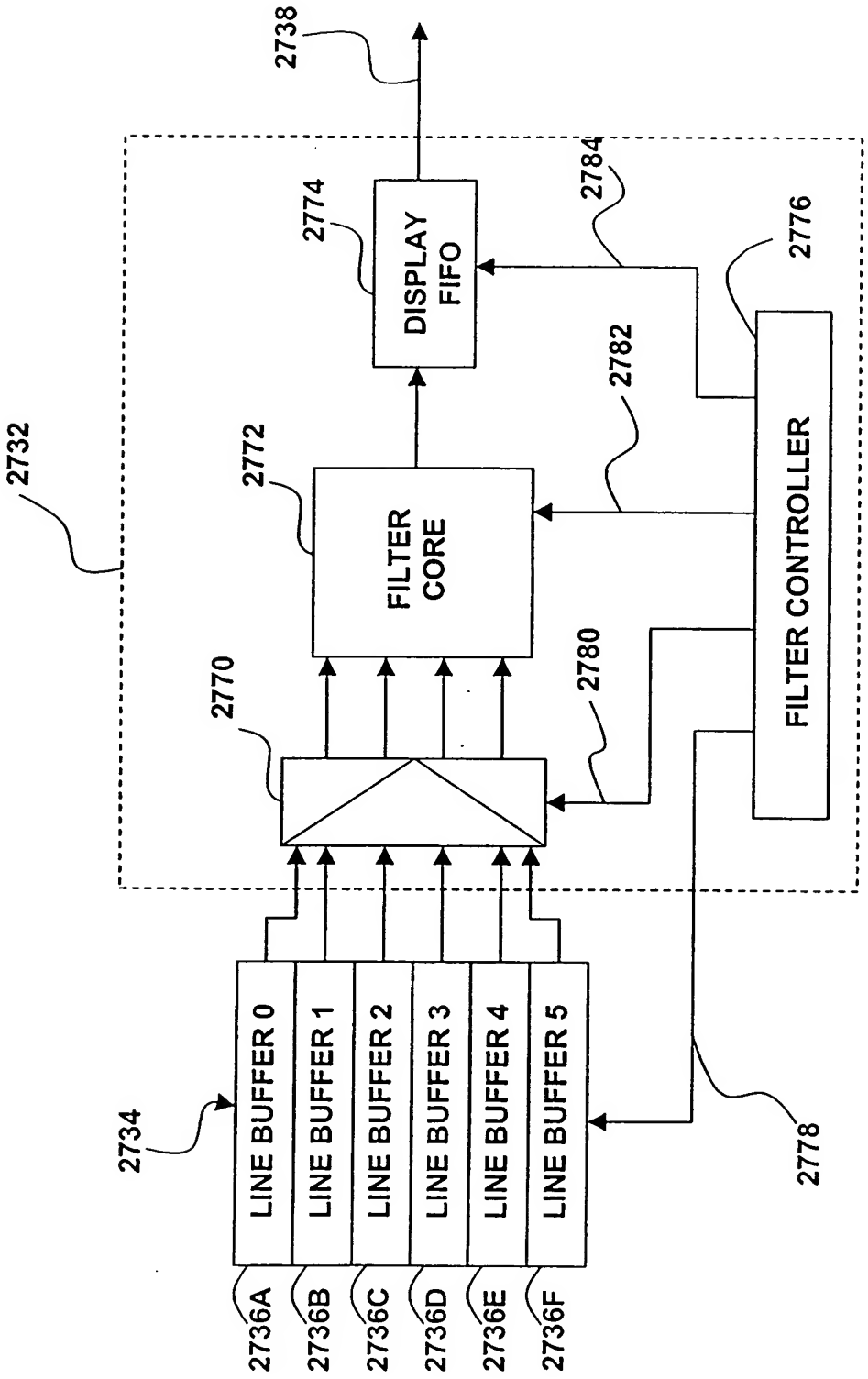
2738
2774
DISPLAY FIFO
2784
2776
2732
2772
FILTER CORE
2782
FILTER CONTROLLER
2770
2780
2734
LINE BUFFER 0
LINE BUFFER 1
LINE BUFFER 2
LINE BUFFER 3
LINE BUFFER 4
LINE BUFFER 5
2778
2736A
2736B
2736C
2736D
2736E
2736F

FIG. 73

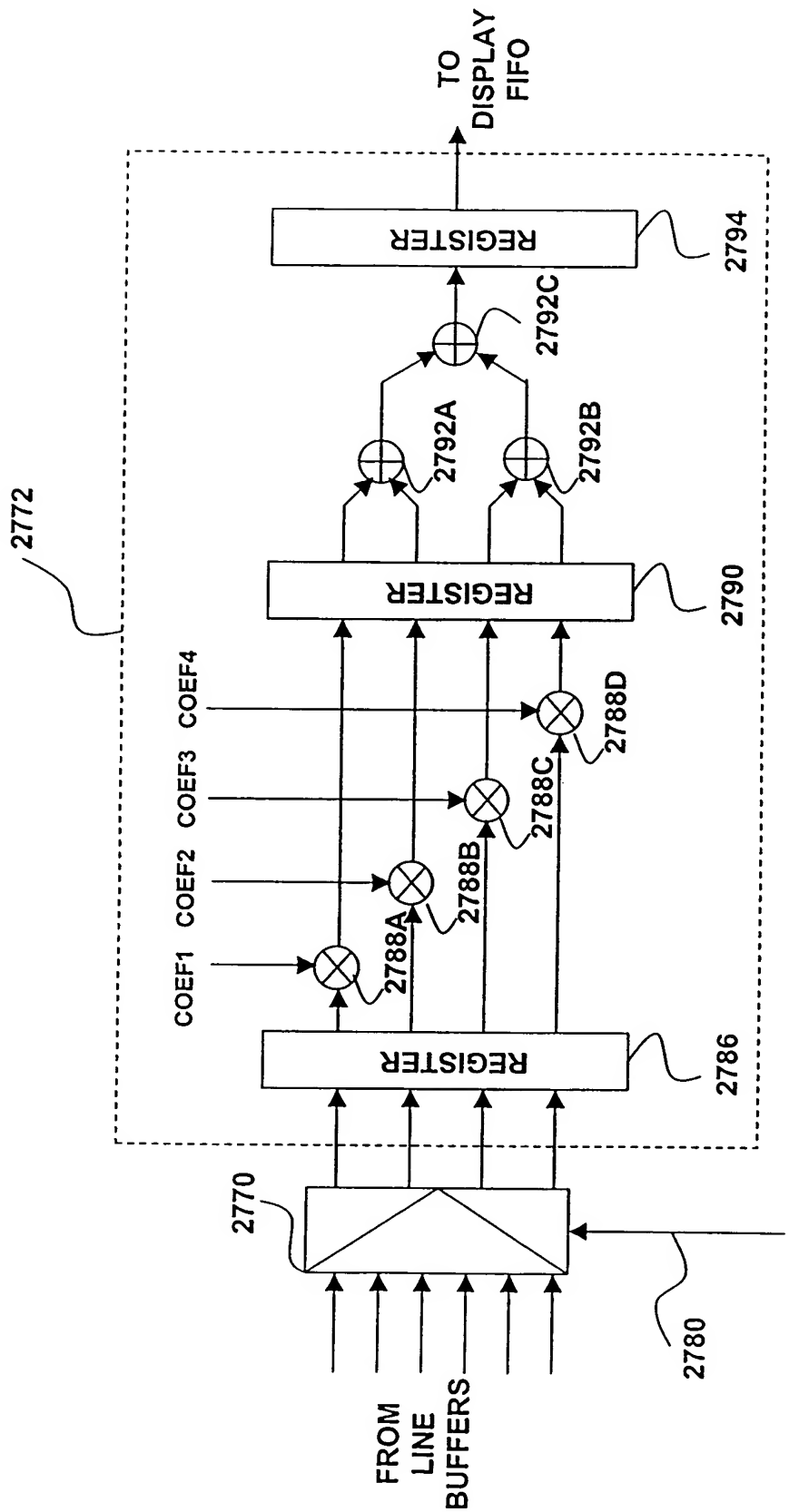
TO DISPLAY FIFO
REGISTER
2794
2792C
2792A
2792B
2772
REGISTER
2790
COEF4
COEF3
COEF2
COEF1
2788D
2788C
2788B
2788A
REGISTER
2786
2770
2780
FROM LINE BUFFERS

FIG. 74

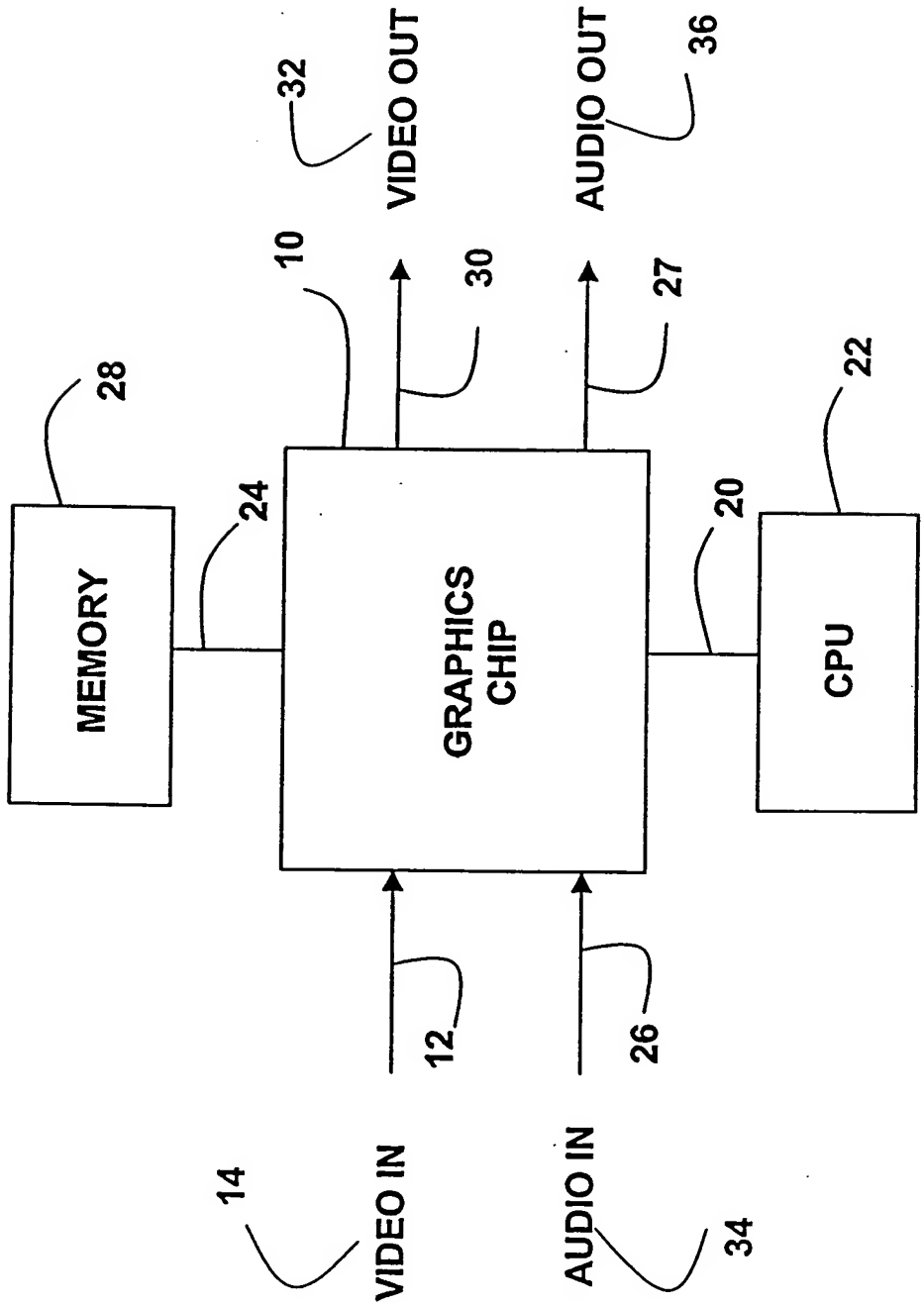
VIDEO OUT
32
AUDIO OUT
36
10
30
27
28
22
24
20
MEMORY
GRAPHICS CHIP
CPU
12
26
14
VIDEO IN
AUDIO IN
34

FIG. 1

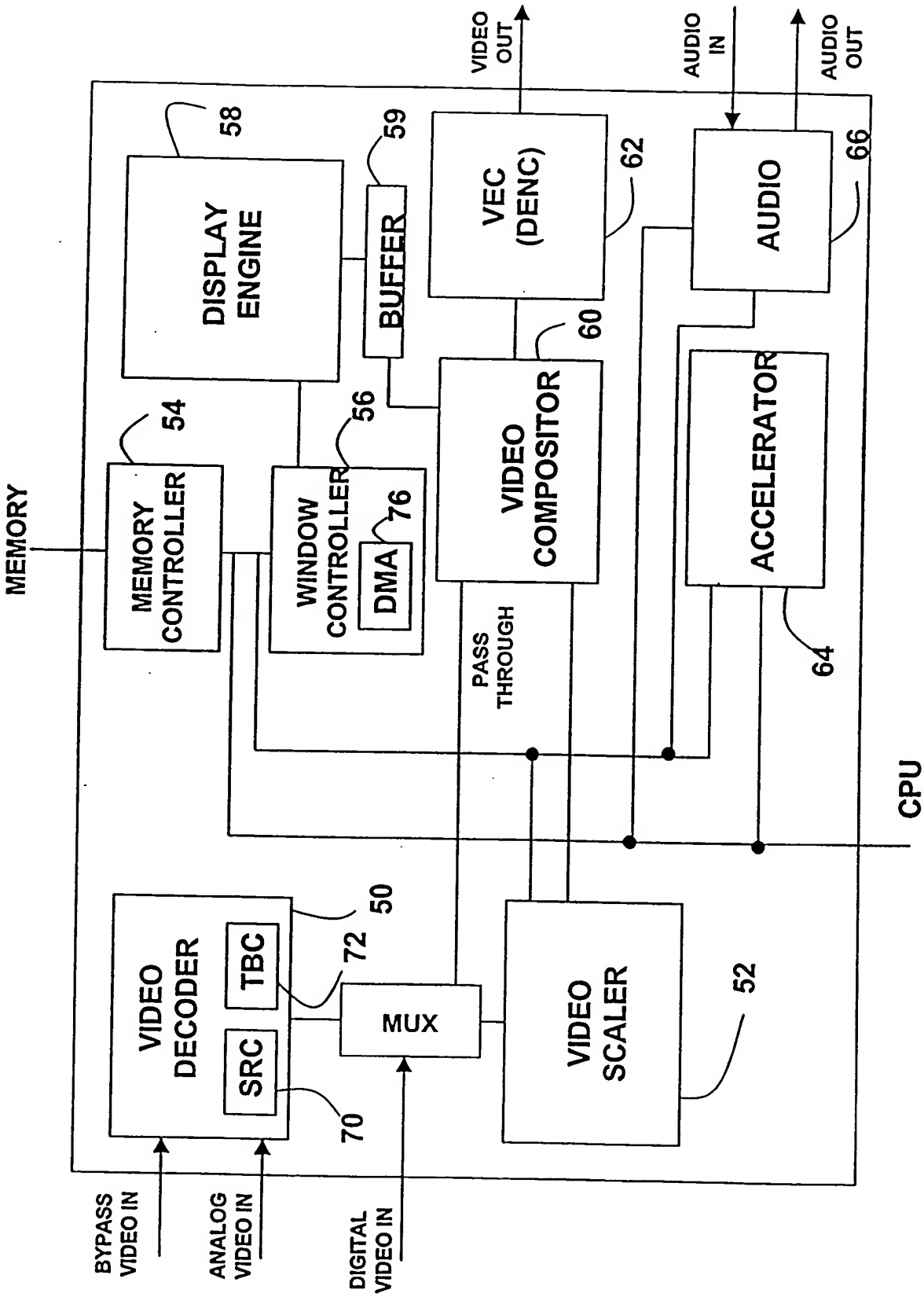
VIDEO OUT
AUDIO IN
AUDIO OUT
DISPLAY ENGINE
58
BUFFER
59
VEC (DENC)
62
AUDIO
66
VIDEO COMPOSITOR
60
ACCELERATOR
64
MEMORY
MEMORY CONTROLLER
54
WINDOW CONTROLLER
56
DMA
76
PASS THROUGH
CPU
VIDEO DECODER
50
TBC
72
SRC
70
MUX
VIDEO SCALER
52
BYPASS VIDEO IN
ANALOG VIDEO IN
DIGITAL VIDEO IN

FIG. 2

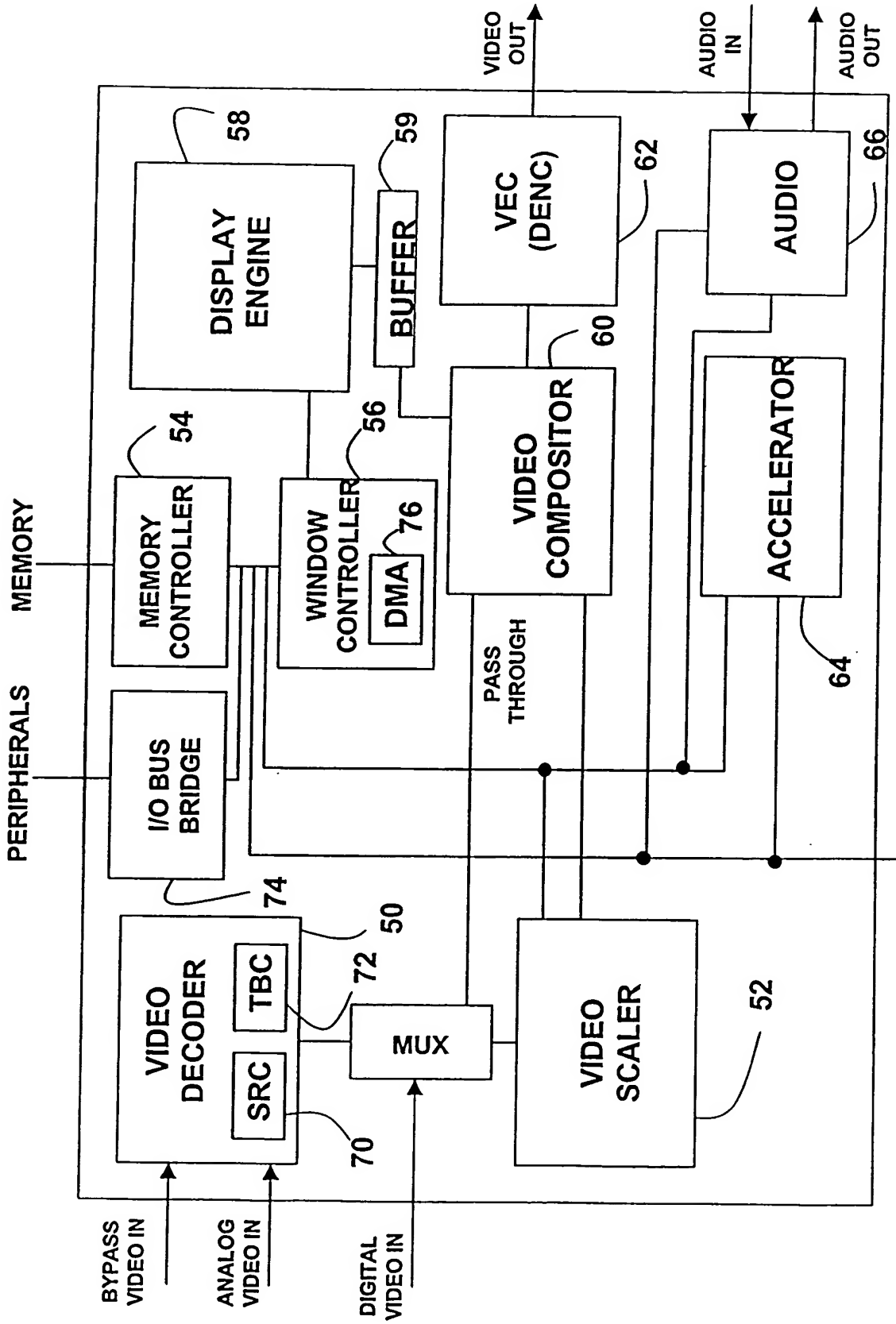
VIDEO OUT
AUDIO IN
AUDIO OUT
DISPLAY ENGINE
58
BUFFER
59
VEC (DENC)
62
AUDIO
66
VIDEO COMPOSITOR
60
ACCELERATOR
64
MEMORY CONTROLLER
54
WINDOW CONTROLLER
56
DMA
76
MEMORY
PERIPHERALS
I/O BUS BRIDGE
74
PASS THROUGH
CPU
VIDEO DECODER
50
TBC
72
SRC
70
MUX
VIDEO SCALER
52
BYPASS VIDEO IN
ANALOG VIDEO IN
DIGITAL VIDEO IN

FIG. 3

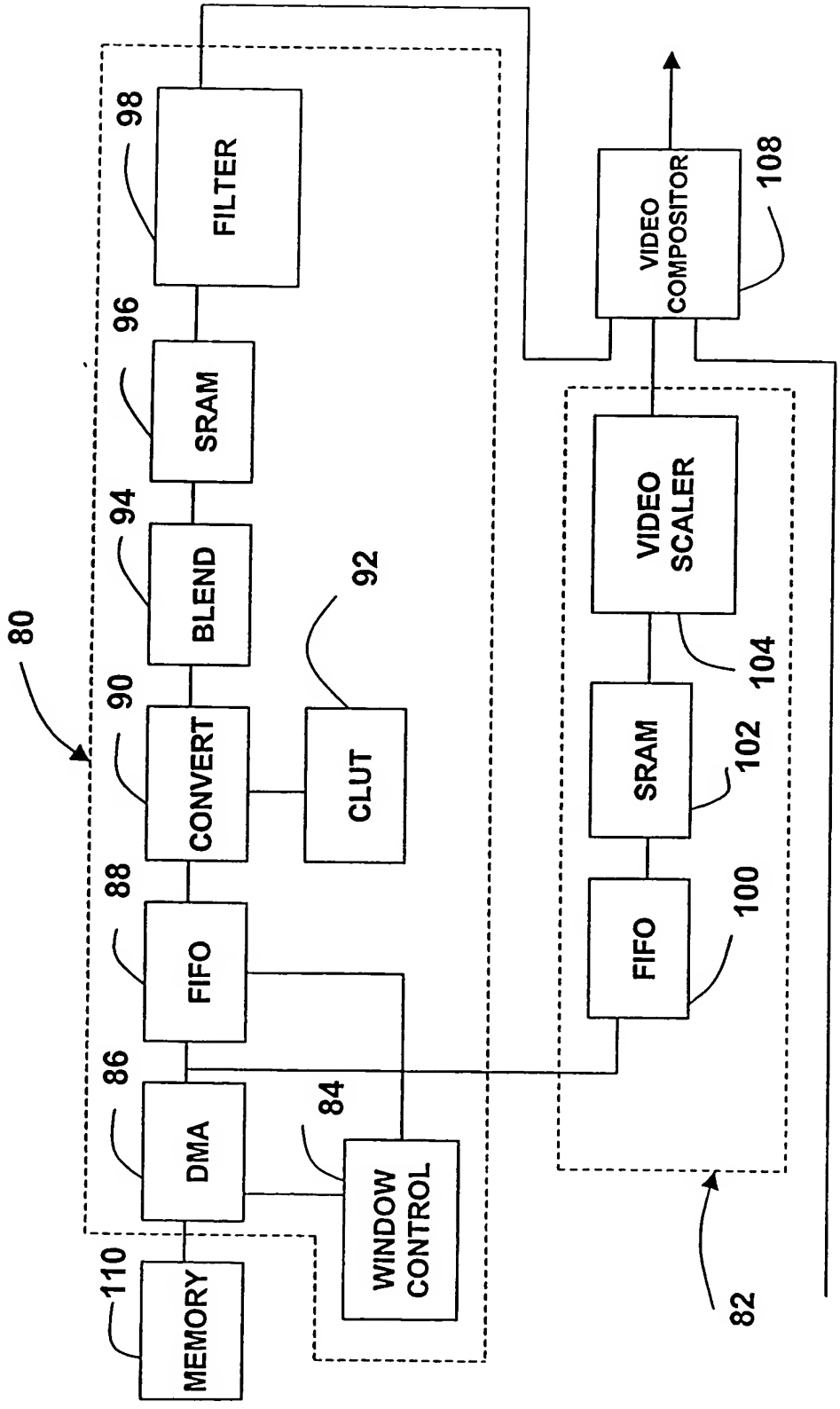
80
82
84
86
88
90
92
94
96
98
100
102
104
108
110
MEMORY
DMA
FIFO
CONVERT
CLUT
BLEND
SRAM
FILTER
WINDOW CONTROL
FIFO
SRAM
VIDEO SCALER
VIDEO COMPOSITOR
PASSTHROUGH VIDEO

FIG. 4

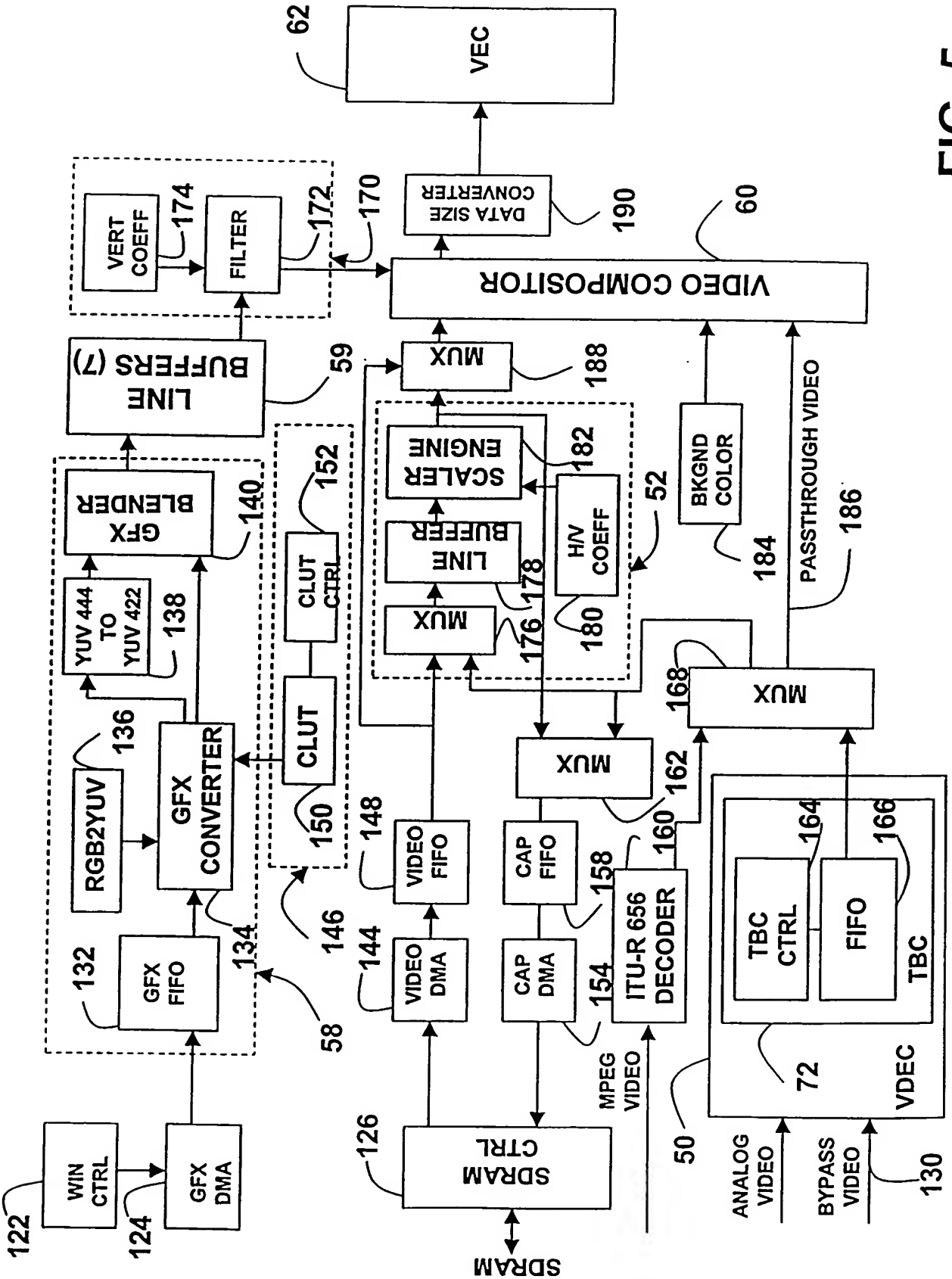
VEC
62
VIDEO COMPOSITOR
60
DATA SIZE CONVERTER
190
VERT COEFF
174
FILTER
172
170
LINE BUFFERS (7)
59
MUX
188
SCALER ENGINE
182
LINE BUFFER
178
MUX
176
H/V COEFF
180
52
BKGND COLOR
184
PASSTHROUGH VIDEO
186
GFX BLENDER
140
CLUT CTRL
152
YUV 444 TO YUV 422
138
CLUT
150
MUX
168
RGB2YUV
136
GFX CONVERTER
VIDEO FIFO
148
CAP FIFO
158
MUX
162
ITU-R 656 DECODER
160
TBC CTRL
164
FIFO
166
TBC
GFX FIFO
132
134
146
VIDEO DMA
144
CAP DMA
154
58
MPEG VIDEO
72
VDEC
50
SDRAM CTRL
126
WIN CTRL
122
GFX DMA
124
ANALOG VIDEO
BYPASS VIDEO
130
SDRAM

FIG. 5

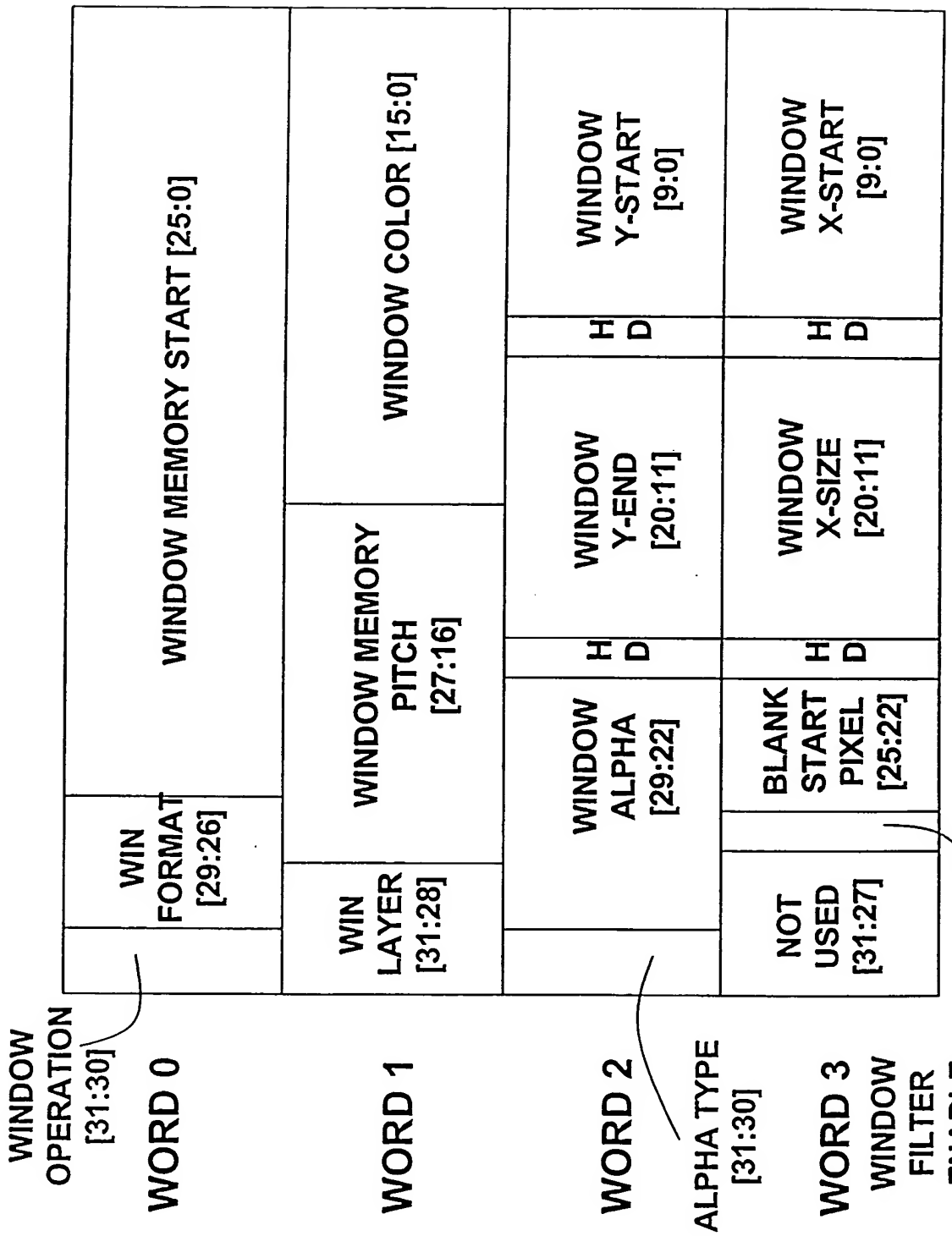
WORD 0
WINDOW MEMORY START [25:0]
WIN FORMAT [29:26]
WINDOW OPERATION [31:30]
WORD 1
WINDOW COLOR [15:0]
WINDOW MEMORY PITCH [27:16]
WIN LAYER [31:28]
WORD 2
WINDOW Y-START [9:0]
HD
WINDOW Y-END [20:11]
HD
WINDOW ALPHA [29:22]
ALPHA TYPE [31:30]
WORD 3
WINDOW X-START [9:0]
HD
WINDOW X-SIZE [20:11]
HD
BLANK START PIXEL [25:22]
NOT USED [31:27]
WINDOW FILTER ENABLE [26]

FIG. 6

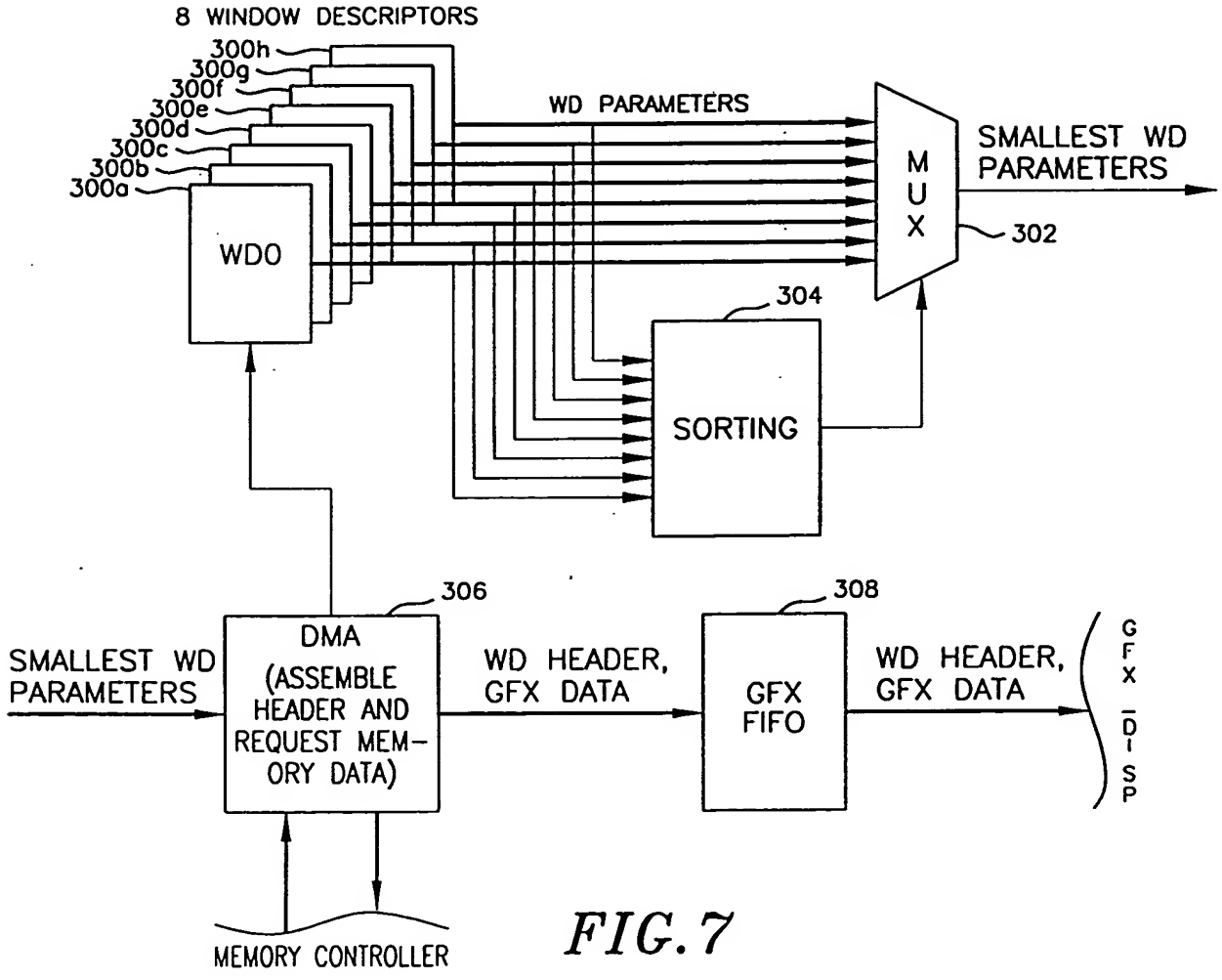
8 WINDOW DESCRIPTORS
300h
300g
300f
300e
300d
300c
300b
300a
WDO
WD PARAMETERS
M
U
X
SMALLEST WD PARAMETERS
302
304
SORTING
306
DMA (ASSEMBLE HEADER AND REQUEST MEMORY DATA)
SMALLEST WD PARAMETERS
WD HEADER, GFX DATA
308
GFX FIFO
WD HEADER, GFX DATA
GFX_DISP
MEMORY CONTROLLER

FIG. 7

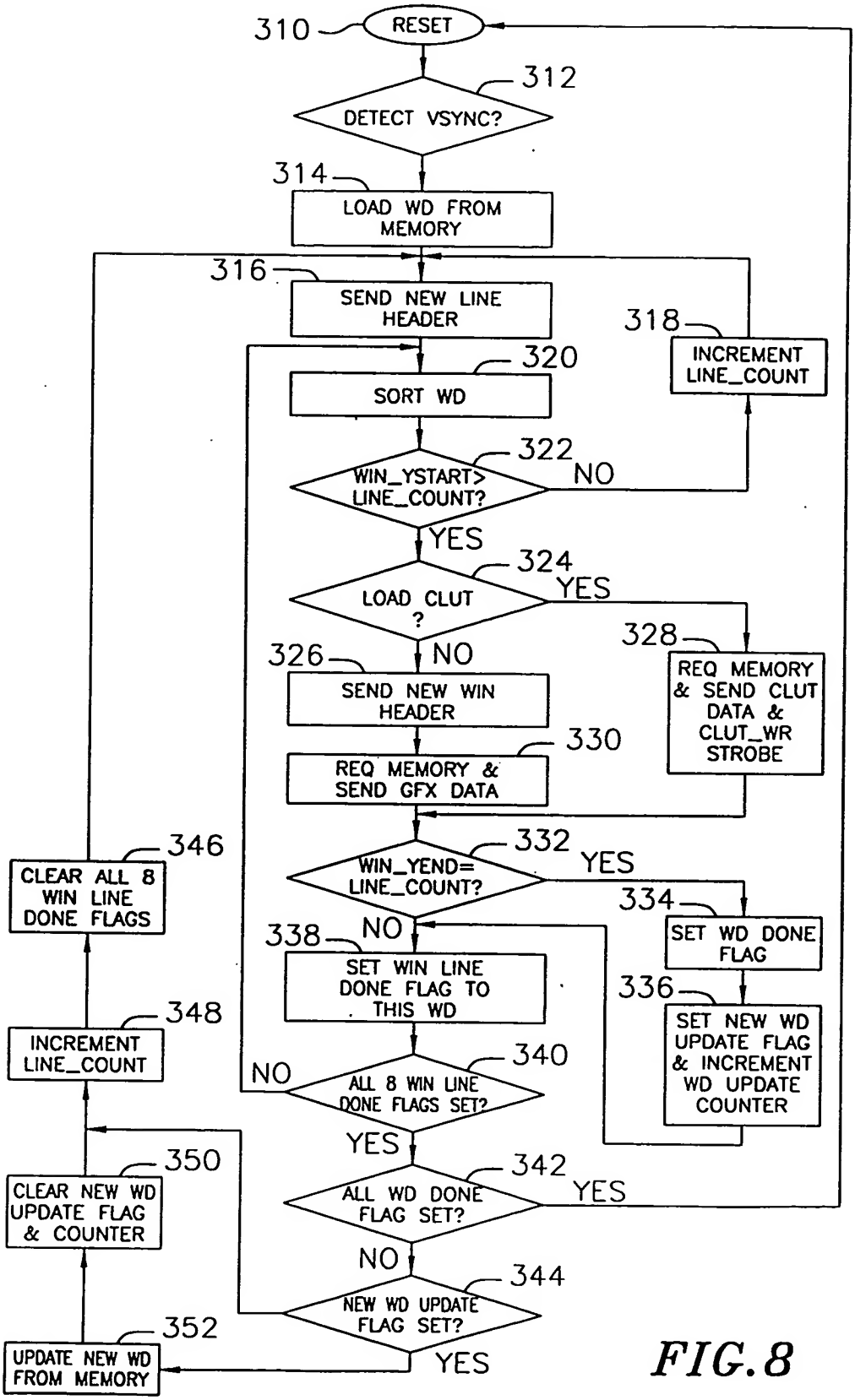
310
RESET
312
DETECT VSYNC?
314
LOAD WD FROM MEMORY
316
SEND NEW LINE HEADER
318
INCREMENT LINE_COUNT
320
SORT WD
322
WIN_YSTART> LINE_COUNT?
NO
YES
324
LOAD CLUT ?
YES
NO
328
REQ MEMORY & SEND CLUT DATA & CLUT_WR STROBE
326
SEND NEW WIN HEADER
330
REQ MEMORY & SEND GFX DATA
332
WIN_YEND= LINE_COUNT?
YES
NO
334
SET WD DONE FLAG
336
SET NEW WD UPDATE FLAG & INCREMENT WD UPDATE COUNTER
338
SET WIN LINE DONE FLAG TO THIS WD
340
ALL 8 WIN LINE DONE FLAGS SET?
NO
YES
342
ALL WD DONE FLAG SET?
YES
NO
344
NEW WD UPDATE FLAG SET?
YES
346
CLEAR ALL 8 WIN LINE DONE FLAGS
348
INCREMENT LINE_COUNT
350
CLEAR NEW WD UPDATE FLAG & COUNTER
352
UPDATE NEW WD FROM MEMORY

FIG.8

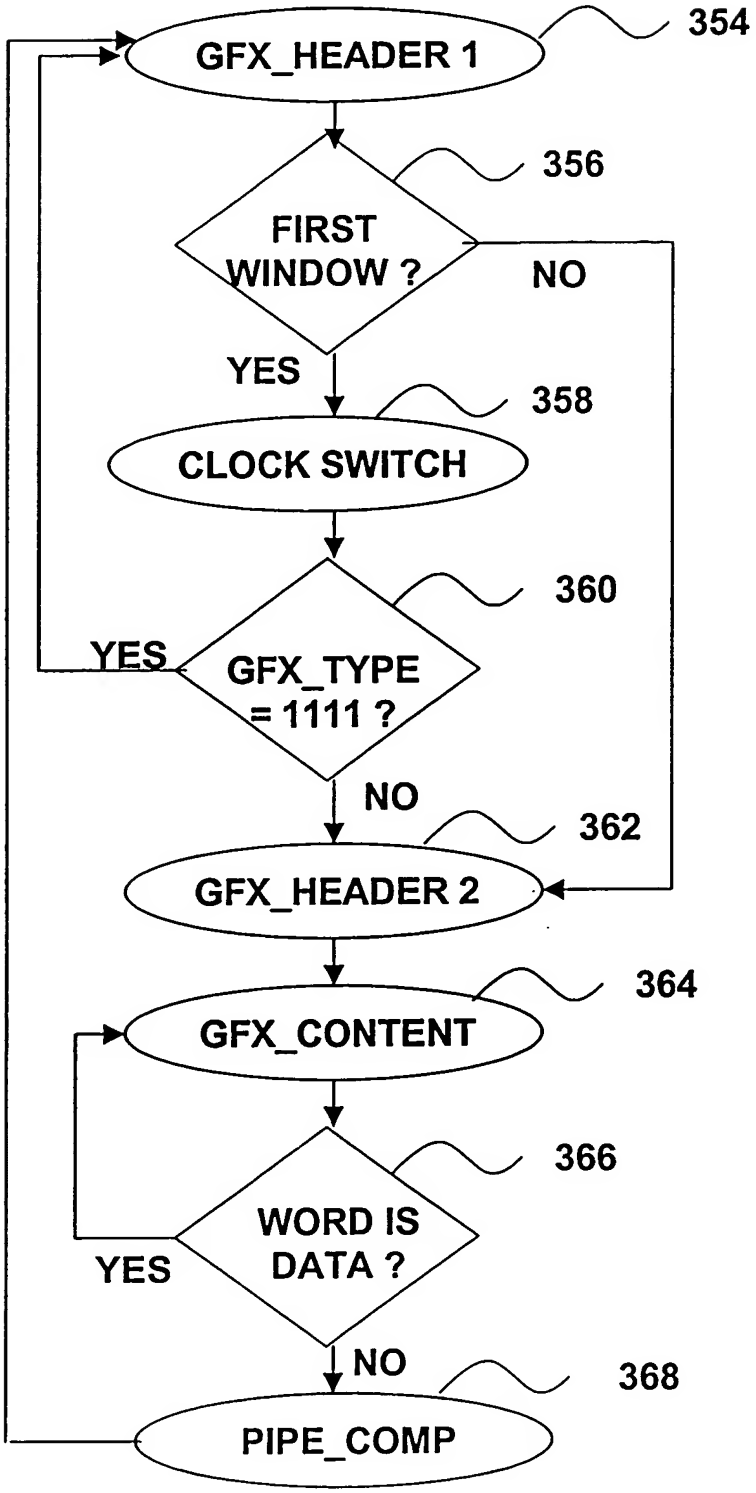
GFX_HEADER 1
354
356
FIRST WINDOW ?
NO
YES
358
CLOCK SWITCH
360
YES
GFX_TYPE = 1111 ?
NO
362
GFX_HEADER 2
364
GFX_CONTENT
366
WORD IS DATA ?
YES
NO
368
PIPE_COMP

FIG. 9

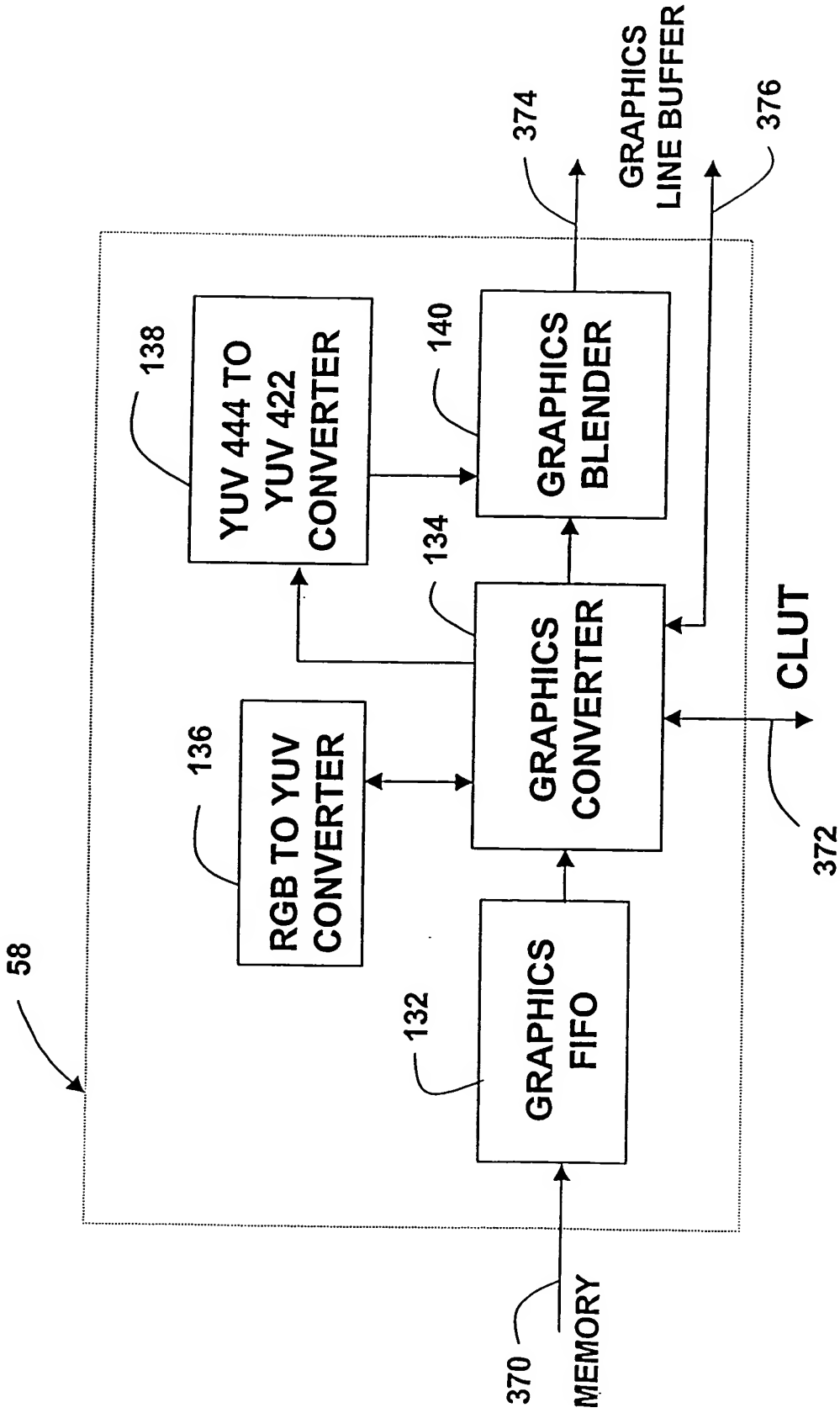
58
370
MEMORY
132
GRAPHICS FIFO
136
RGB TO YUV CONVERTER
134
GRAPHICS CONVERTER
372
CLUT
138
YUV 444 TO YUV 422 CONVERTER
140
GRAPHICS BLENDER
374
376
GRAPHICS LINE BUFFER

FIG. 10

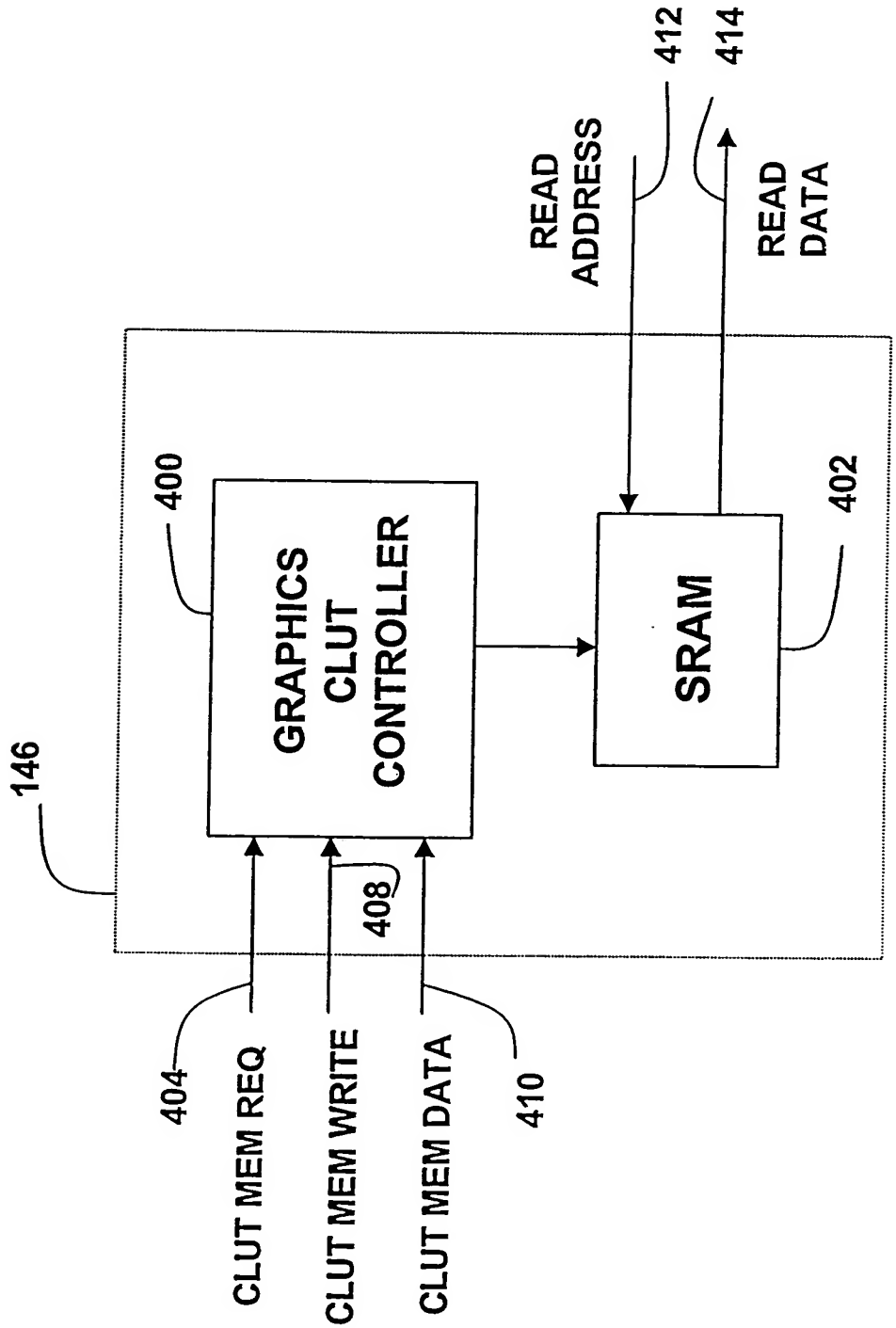
READ ADDRESS
READ DATA
412
414
400
GRAPHICS CLUT CONTROLLER
SRAM
402
146
408
404
CLUT MEM REQ
CLUT MEM WRITE
CLUT MEM DATA
410

FIG. 11

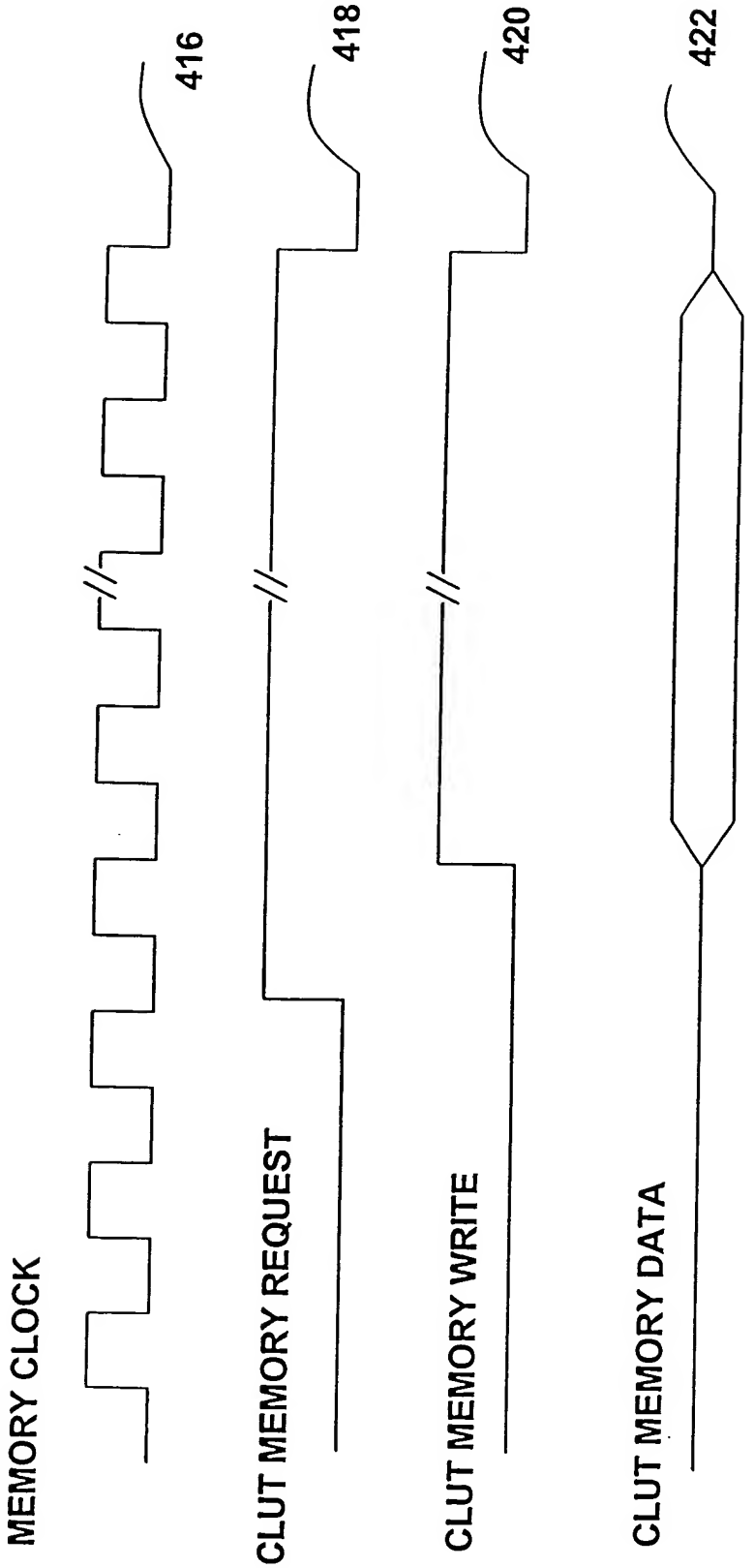
MEMORY CLOCK
CLUT MEMORY REQUEST
CLUT MEMORY WRITE
CLUT MEMORY DATA
416
418
420
422

FIG. 12

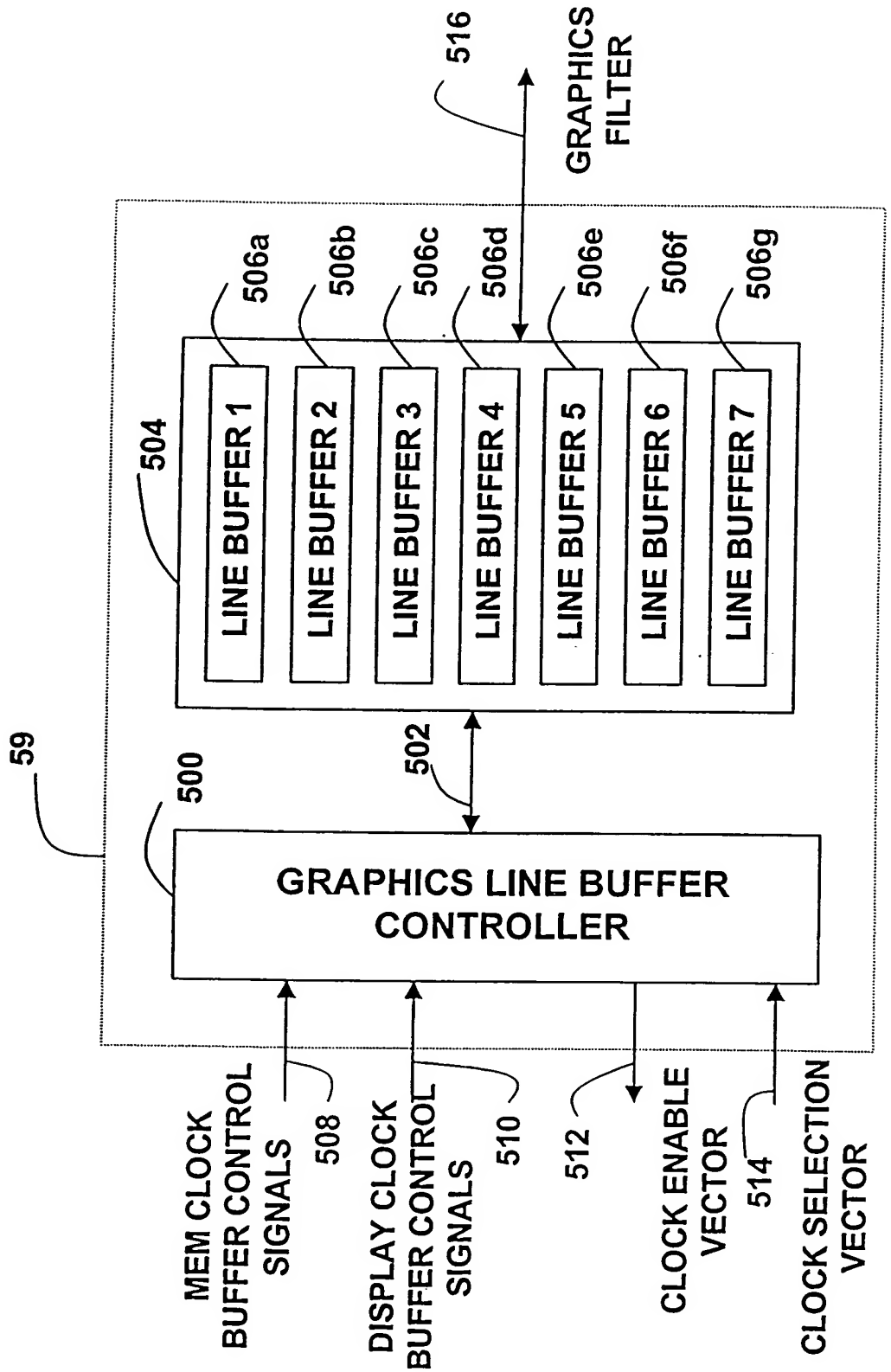
59
500
GRAPHICS LINE BUFFER CONTROLLER
502
504
LINE BUFFER 1
LINE BUFFER 2
LINE BUFFER 3
LINE BUFFER 4
LINE BUFFER 5
LINE BUFFER 6
LINE BUFFER 7
506a
506b
506c
506d
506e
506f
506g
516
GRAPHICS FILTER
MEM CLOCK BUFFER CONTROL SIGNALS
508
DISPLAY CLOCK BUFFER CONTROL SIGNALS
510
512
CLOCK ENABLE VECTOR
514
CLOCK SELECTION VECTOR

FIG. 13

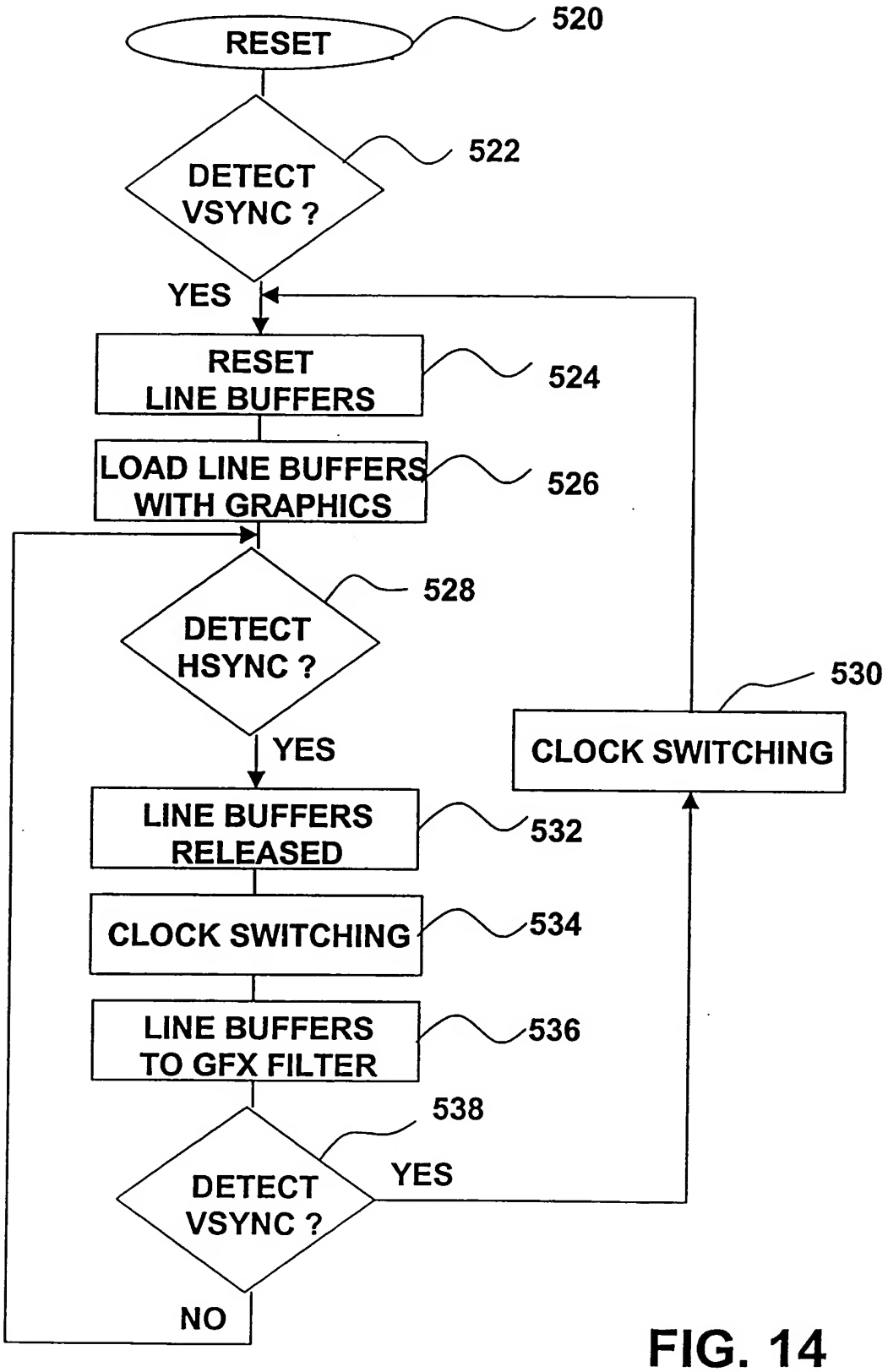
RESET
520
DETECT VSYNC ?
522
YES
RESET LINE BUFFERS
524
LOAD LINE BUFFERS WITH GRAPHICS
526
DETECT HSYNC ?
528
YES
LINE BUFFERS RELEASED
532
CLOCK SWITCHING
534
LINE BUFFERS TO GFX FILTER
536
DETECT VSYNC ?
538
YES
NO
CLOCK SWITCHING
530

FIG. 14

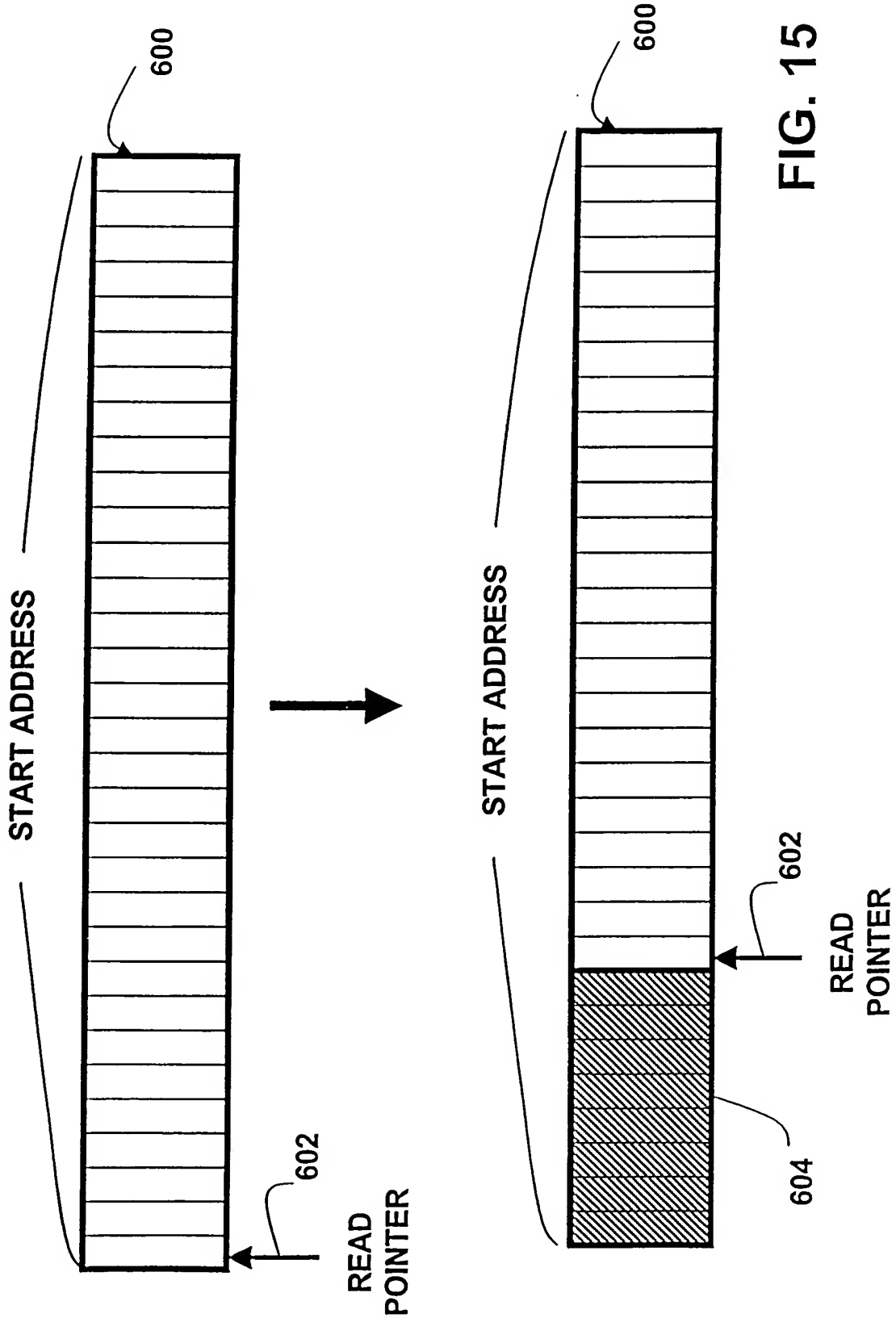
600
START ADDRESS
602
READ POINTER
600
START ADDRESS
602
READ POINTER
604

FIG. 15

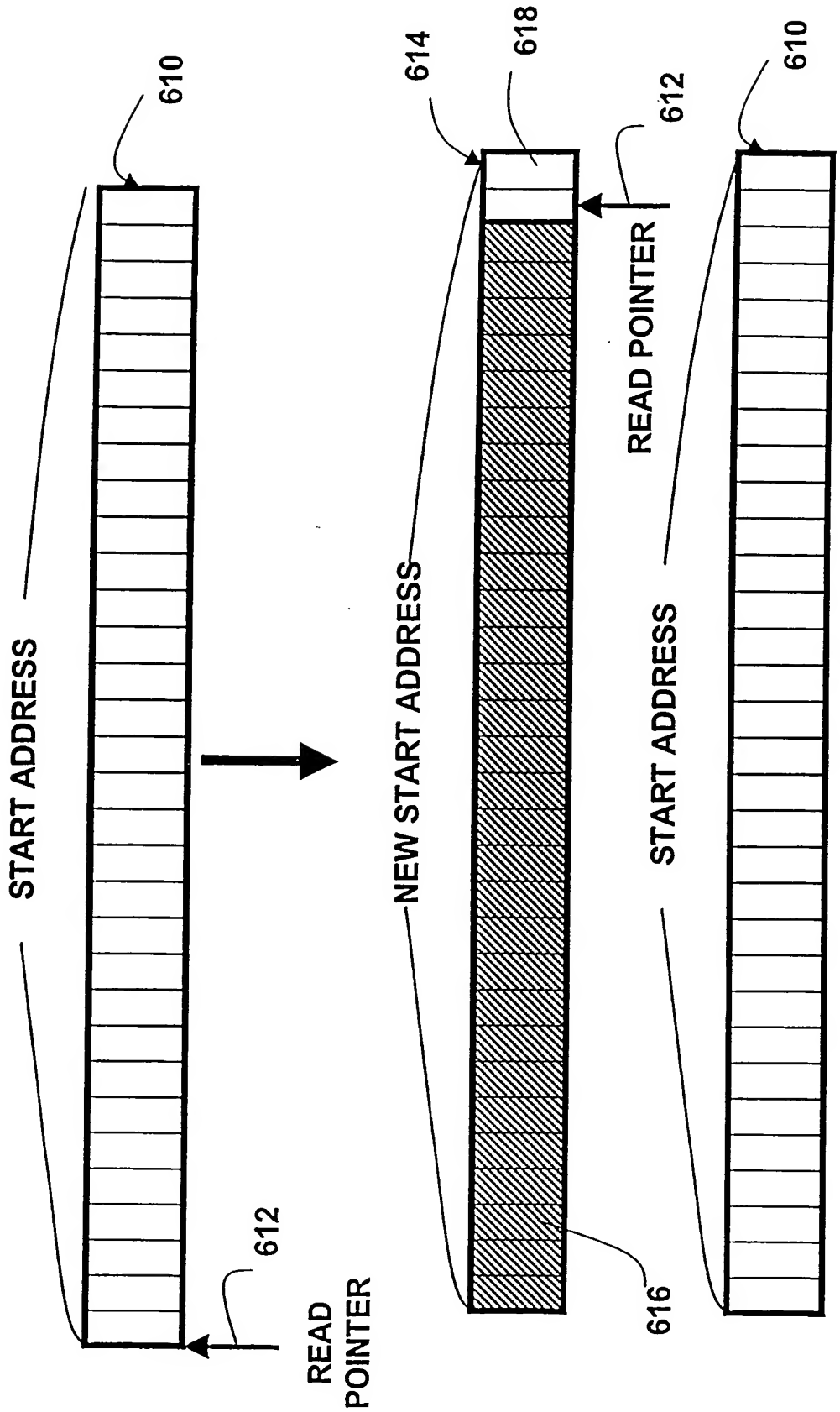
610
START ADDRESS
612
READ POINTER
614
618
NEW START ADDRESS
612
READ POINTER
610
START ADDRESS
616

FIG. 16

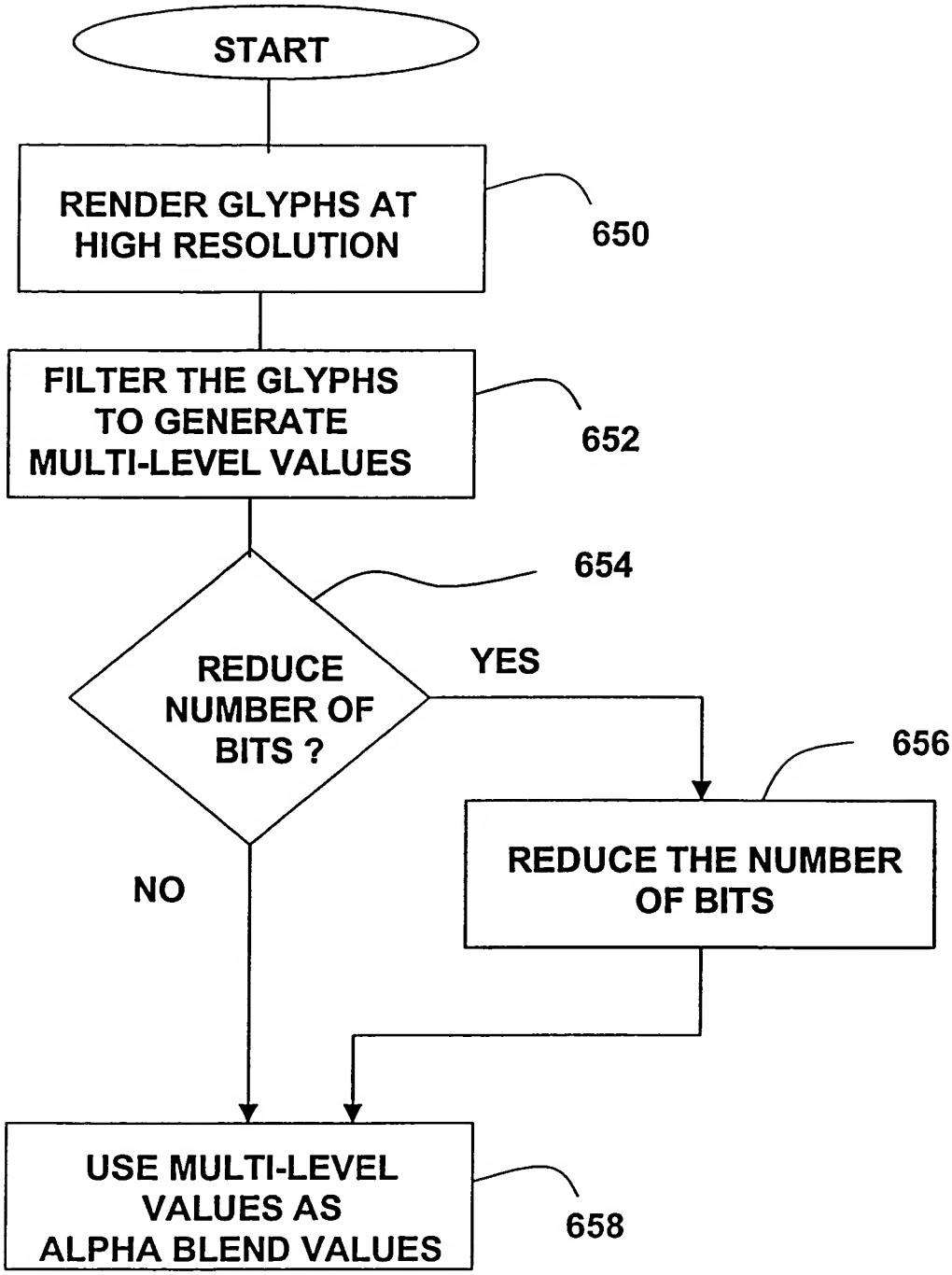
START
RENDER GLYPHS AT HIGH RESOLUTION
650
FILTER THE GLYPHS TO GENERATE MULTI-LEVEL VALUES
652
654
REDUCE NUMBER OF BITS ?
YES
NO
656
REDUCE THE NUMBER OF BITS
USE MULTI-LEVEL VALUES AS ALPHA BLEND VALUES
658

FIG. 17

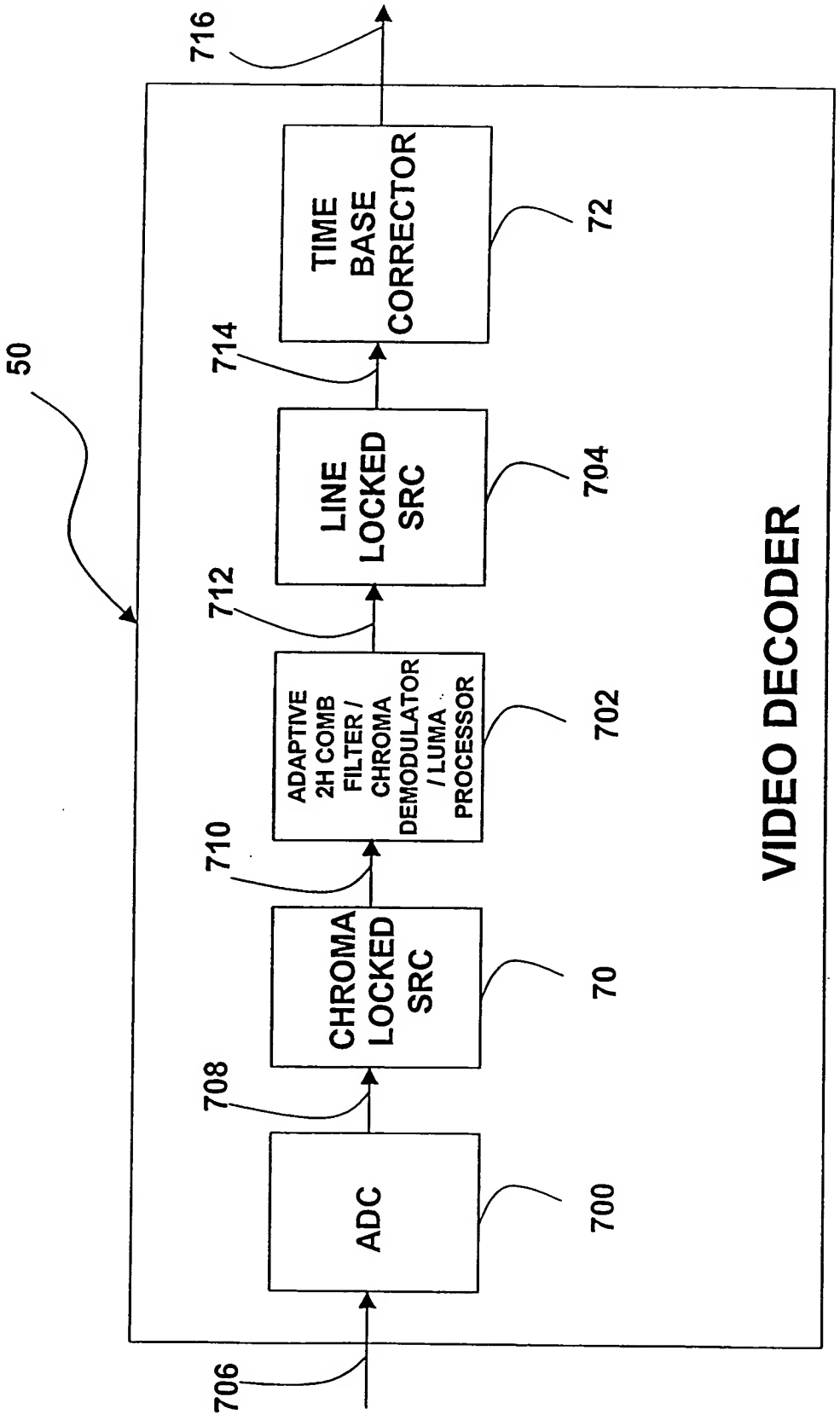
50
VIDEO DECODER
ADC
700
CHROMA LOCKED SRC
70
ADAPTIVE 2H COMB FILTER / CHROMA DEMODULATOR / LUMA PROCESSOR
702
LINE LOCKED SRC
704
TIME BASE CORRECTOR
72
706
708
710
712
714
716

FIG. 18

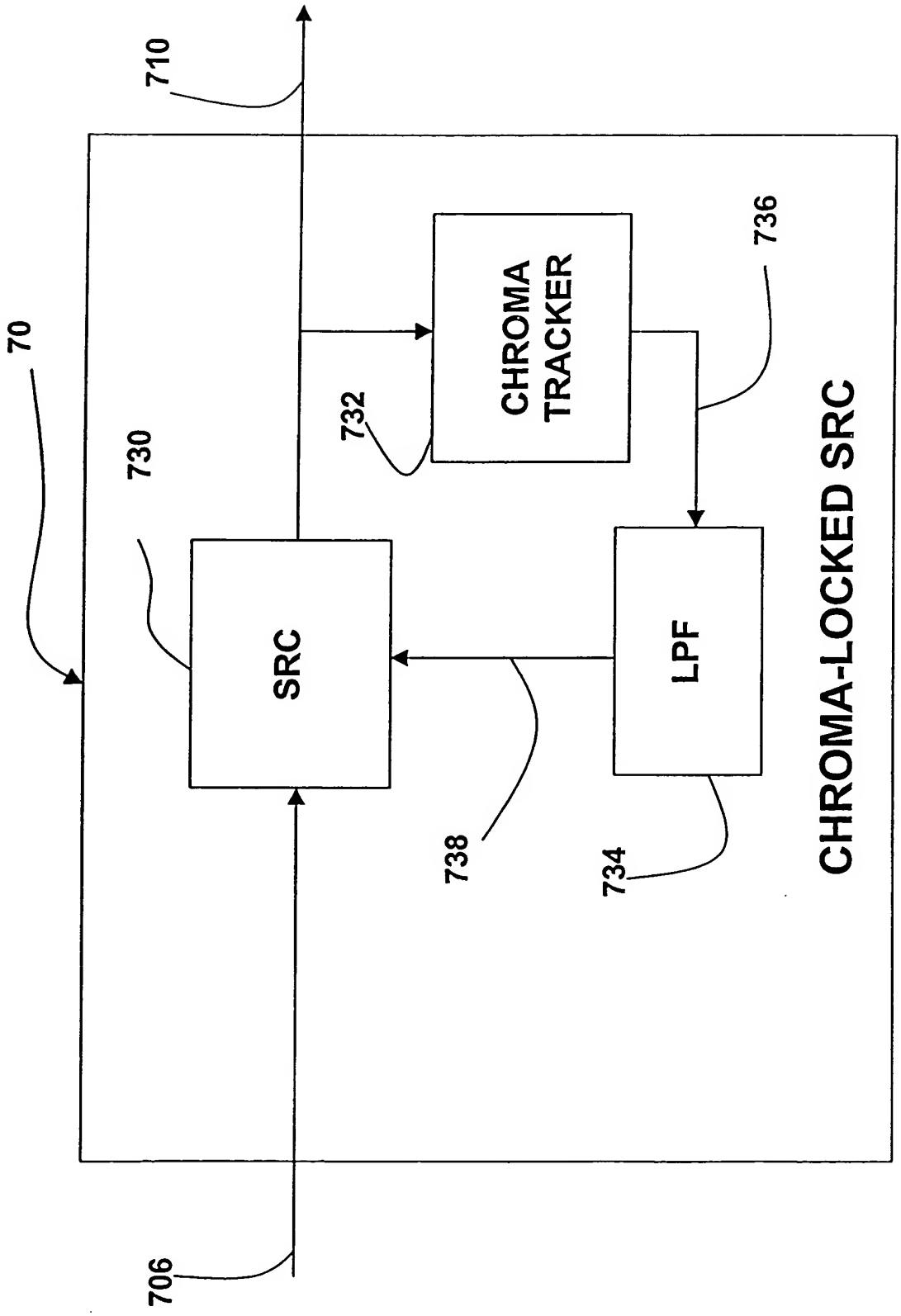
710
70
730
732
CHROMA TRACKER
736
SRC
LPF
738
734
CHROMA-LOCKED SRC
706

FIG. 19

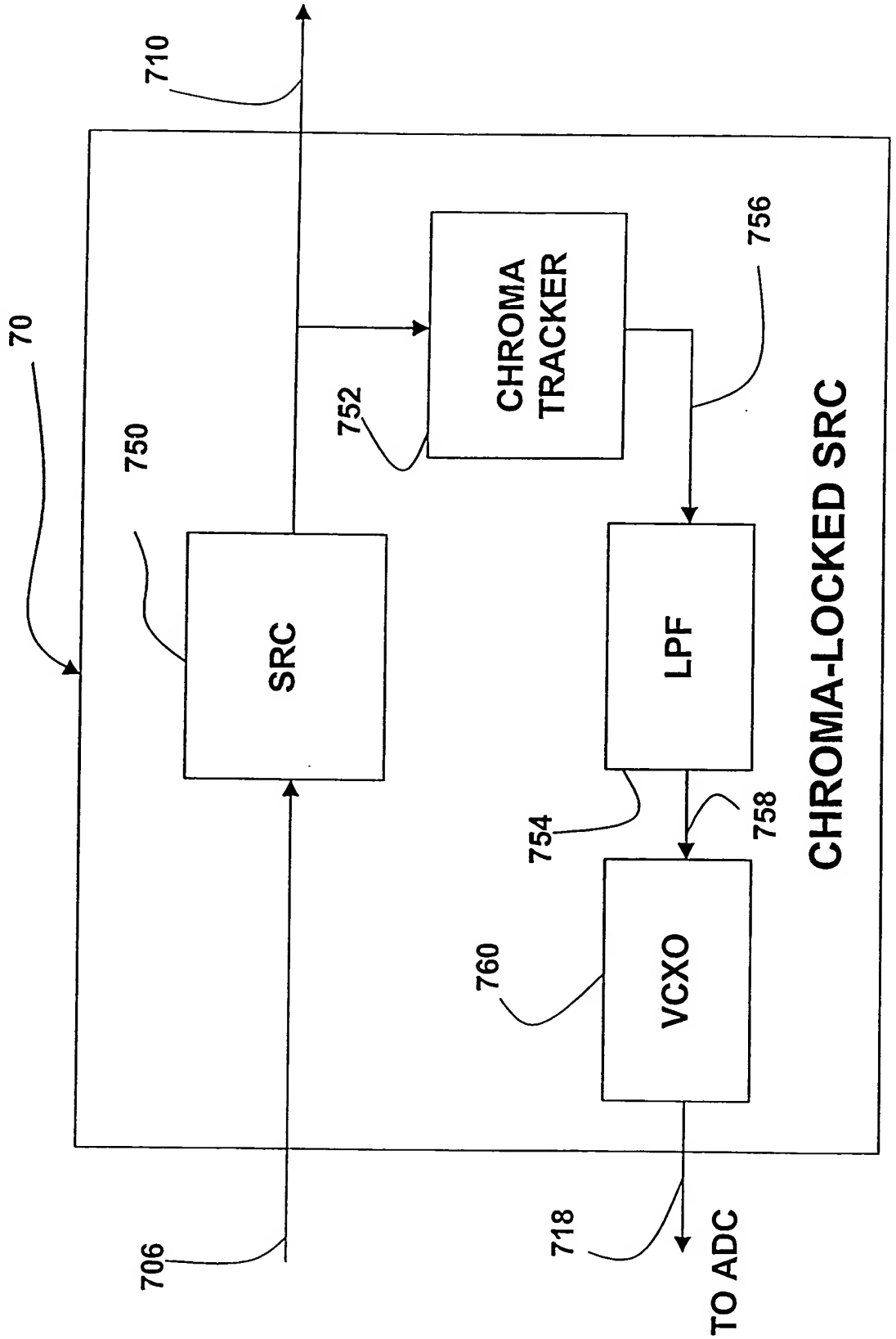
710
70
750
752
CHROMA TRACKER
756
SRC
LPF
754
758
CHROMA-LOCKED SRC
760
VCXO
706
718
TO ADC

FIG. 20

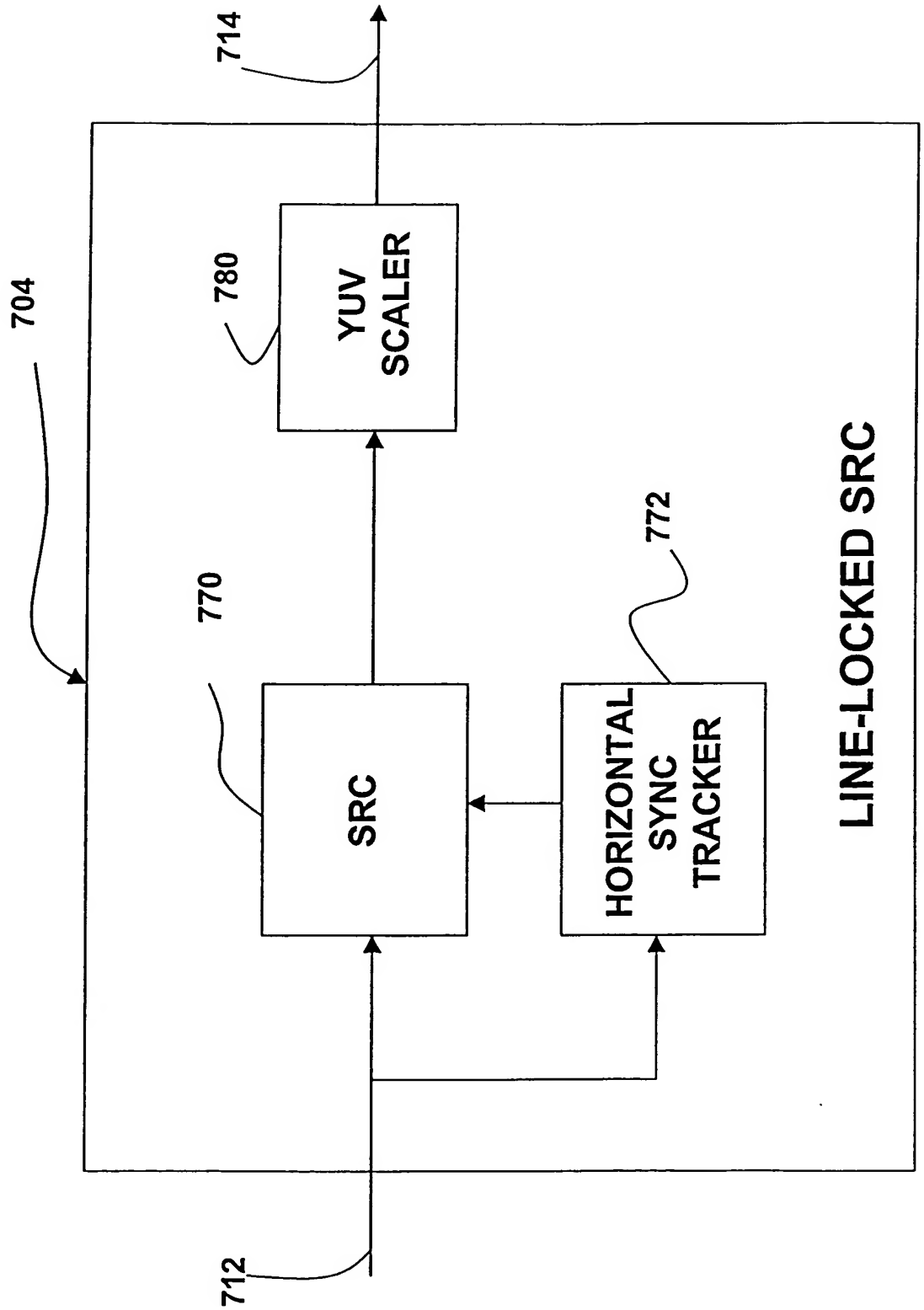
714
704
780
YUV SCALER
770
772
SRC
HORIZONTAL SYNC TRACKER
LINE-LOCKED SRC
712

FIG. 21

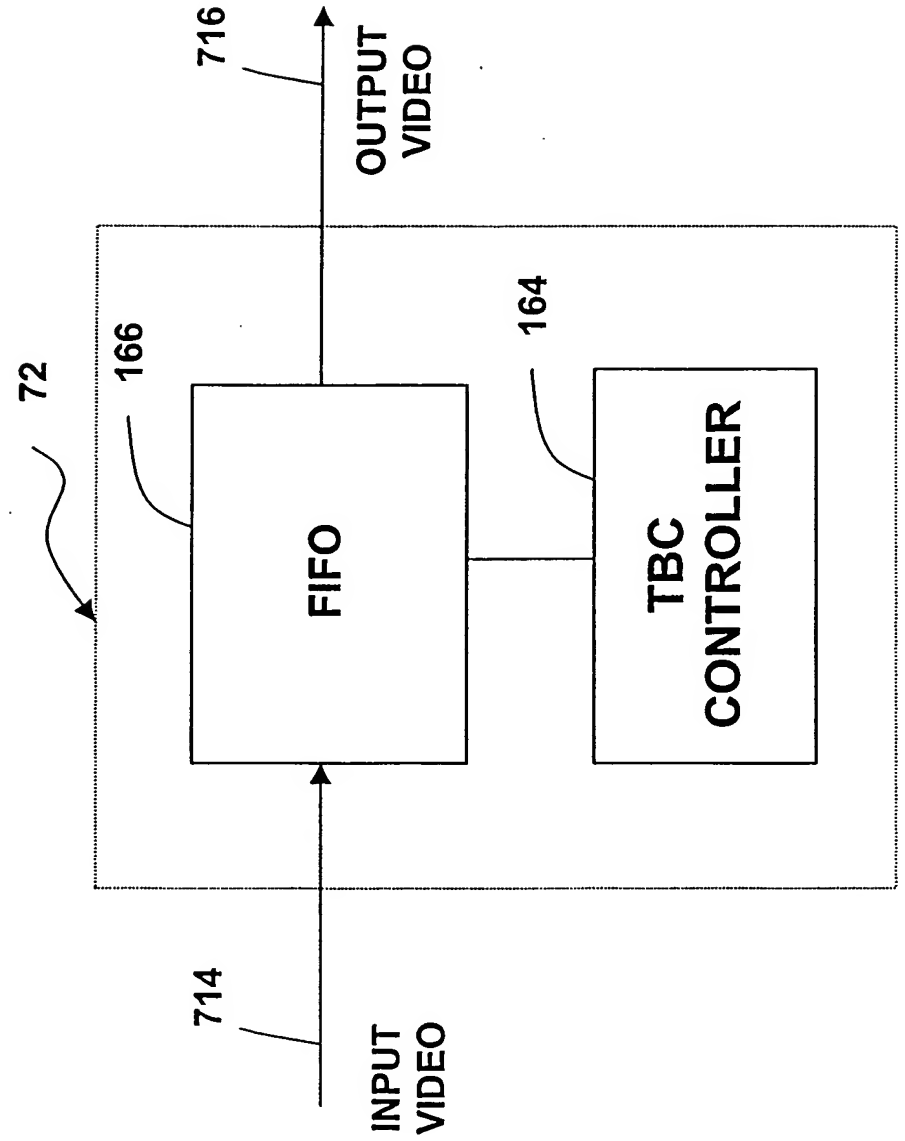
716
OUTPUT VIDEO
72
166
164
FIFO
TBC CONTROLLER
714
INPUT VIDEO

FIG. 22

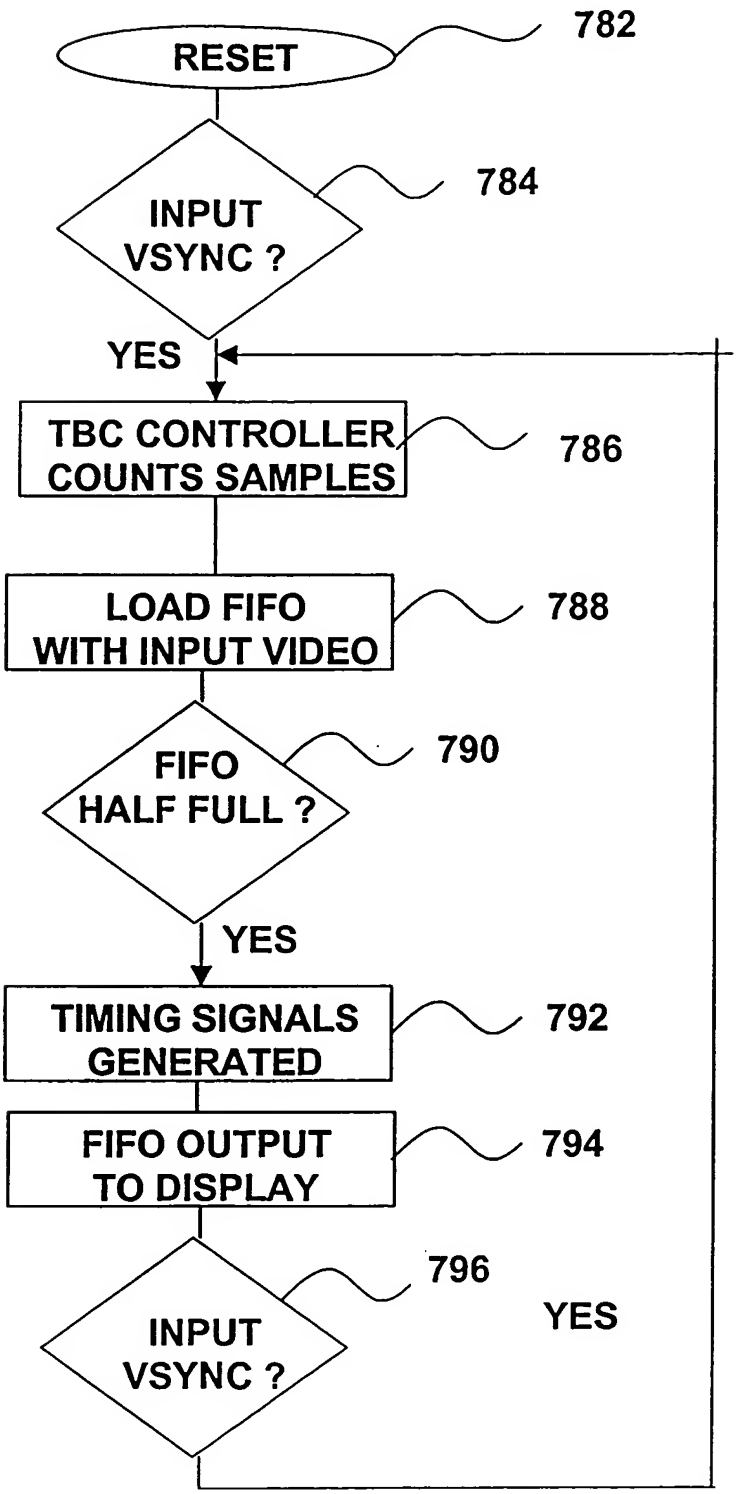
RESET
782
INPUT VSYNC ?
784
YES
TBC CONTROLLER COUNTS SAMPLES
786
LOAD FIFO WITH INPUT VIDEO
788
FIFO HALF FULL ?
790
YES
TIMING SIGNALS GENERATED
792
FIFO OUTPUT TO DISPLAY
794
INPUT VSYNC ?
796
YES

FIG. 23

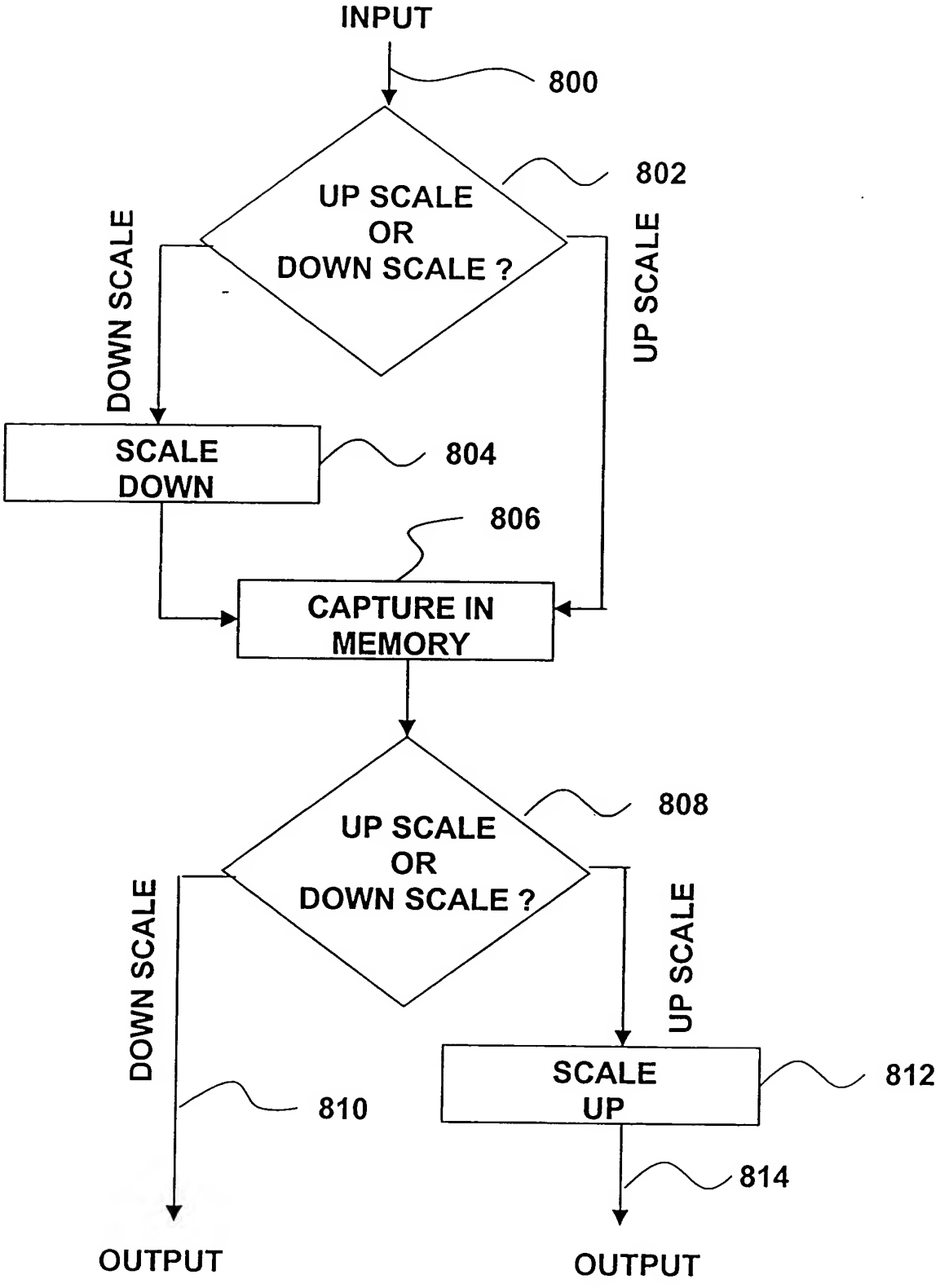
INPUT
800
UP SCALE OR DOWN SCALE ?
802
DOWN SCALE
UP SCALE
SCALE DOWN
804
806
CAPTURE IN MEMORY
UP SCALE OR DOWN SCALE ?
808
DOWN SCALE
UP SCALE
SCALE UP
812
810
814
OUTPUT
OUTPUT

FIG. 24

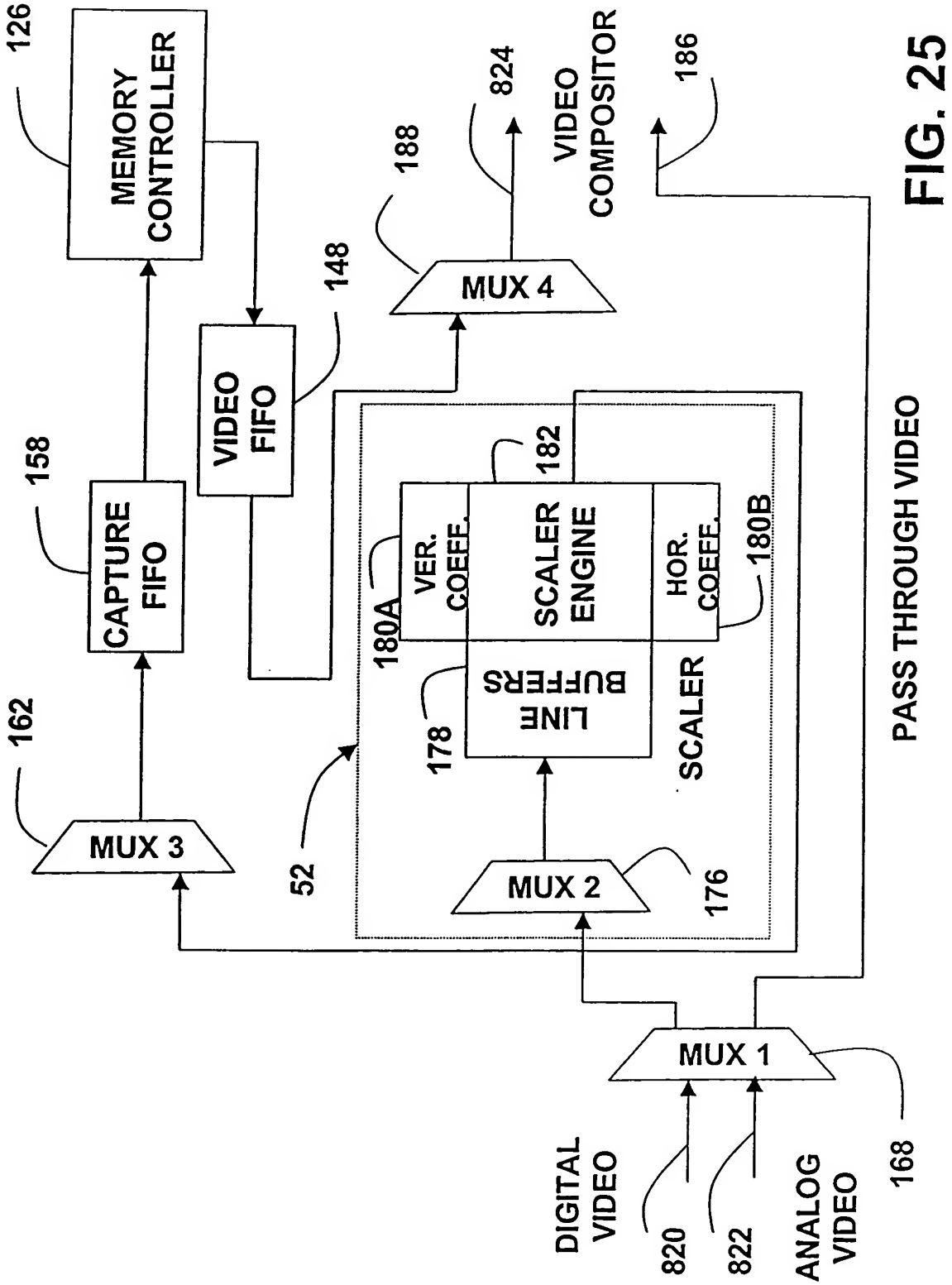
126
MEMORY CONTROLLER
824
VIDEO COMPOSITOR
186
188
148
MUX 4
VIDEO FIFO
158
CAPTURE FIFO
182
VER. COEFF.
SCALER ENGINE
HOR. COEFF.
180B
180A
LINE BUFFERS
178
SCALER
162
MUX 3
52
MUX 2
176
PASS THROUGH VIDEO
MUX 1
DIGITAL VIDEO
820
822
ANALOG VIDEO
168

FIG. 25

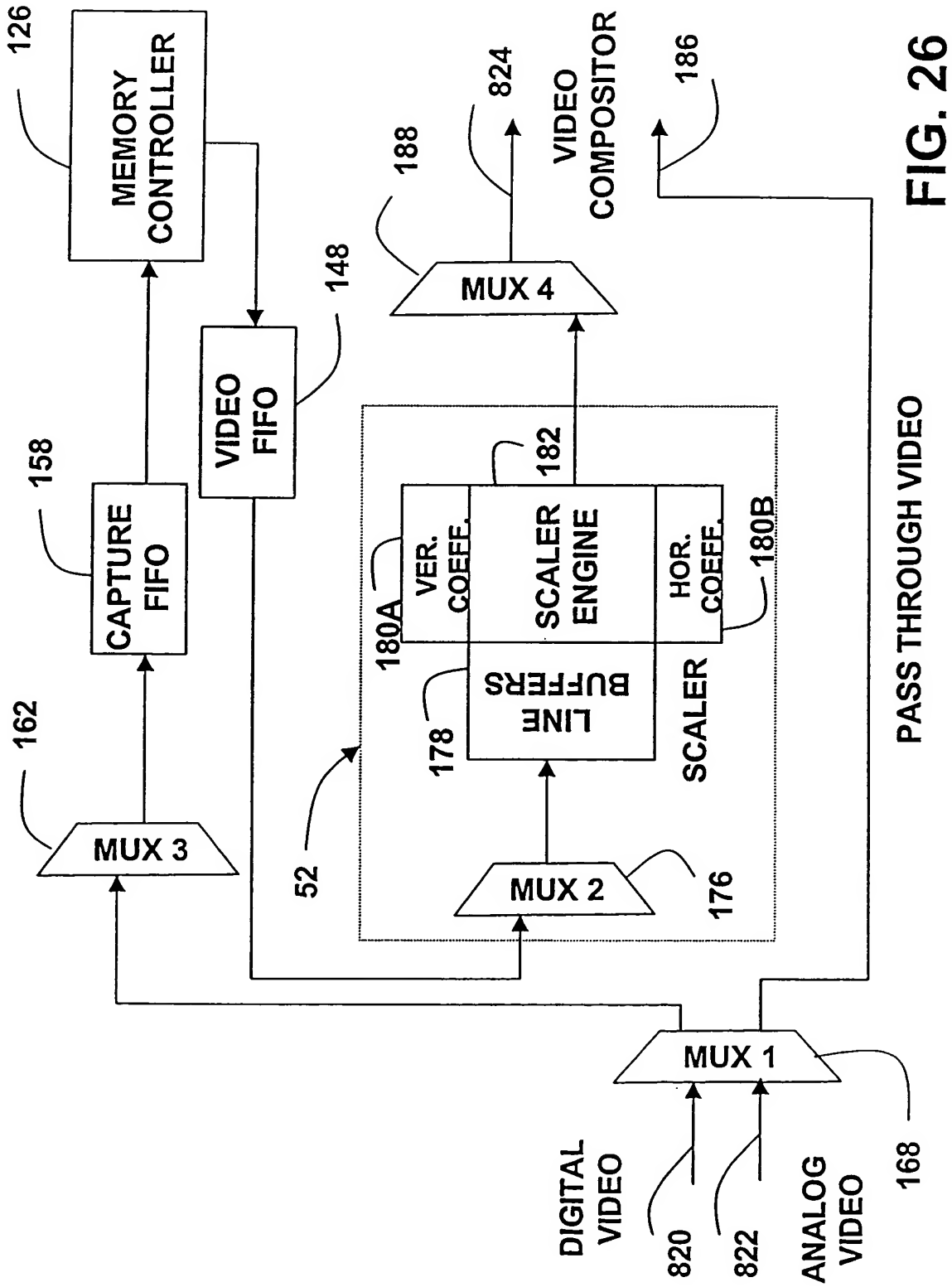
126
MEMORY CONTROLLER
148
VIDEO FIFO
158
CAPTURE FIFO
162
MUX 3
52
188
824
VIDEO COMPOSITOR
186
MUX 4
182
180A
VER. COEFF.
SCALER ENGINE
HOR. COEFF.
180B
178
LINE BUFFERS
SCALER
MUX 2
176
PASS THROUGH VIDEO
MUX 1
168
DIGITAL VIDEO
820
822
ANALOG VIDEO

FIG. 26

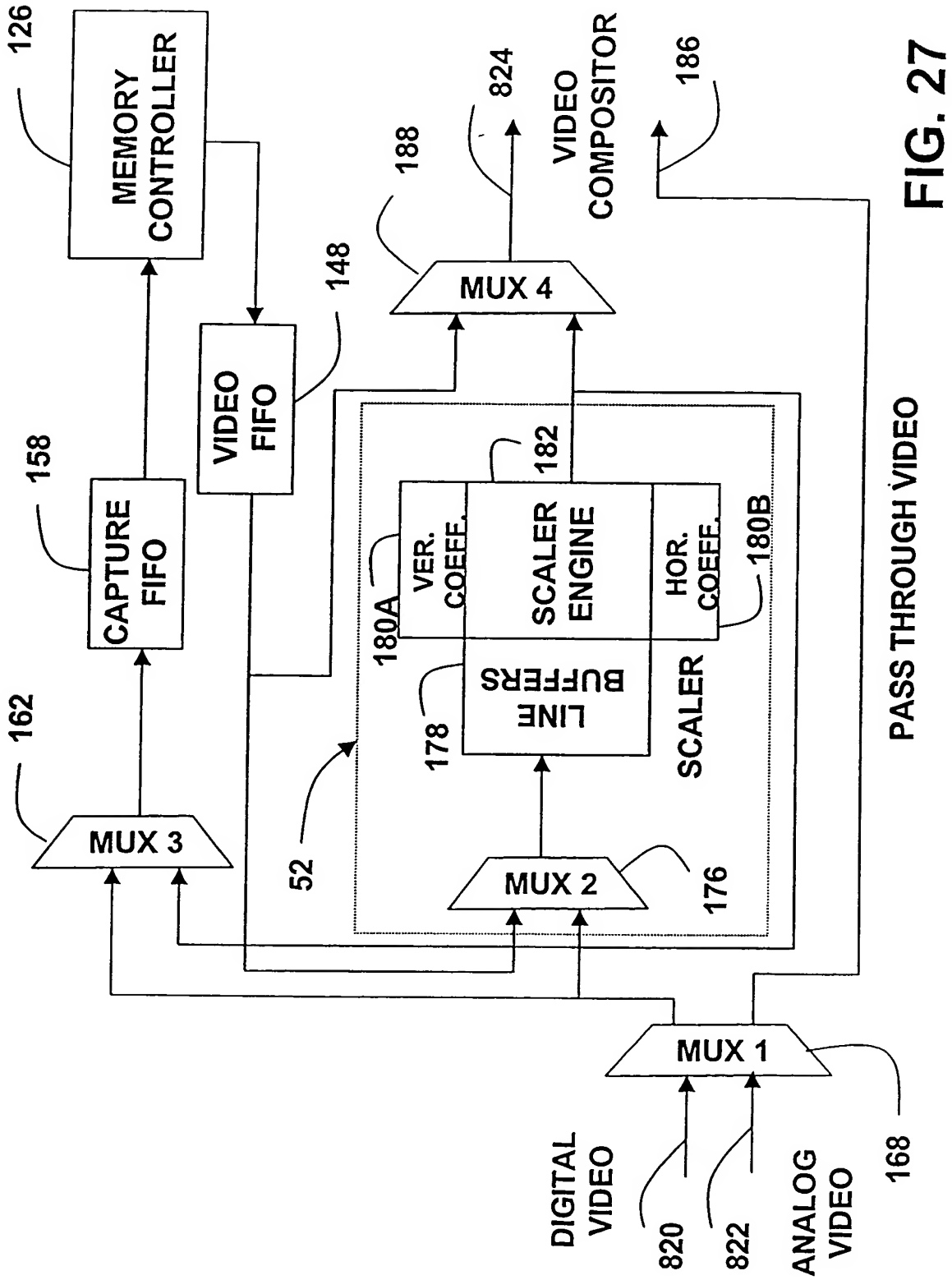
126
MEMORY CONTROLLER
824
VIDEO COMPOSITOR
186
188
148
MUX 4
VIDEO FIFO
158
182
CAPTURE FIFO
VER. COEFF.
SCALER ENGINE
HOR. COEFF.
180B
180A
LINE BUFFERS
178
SCALER
162
MUX 3
52
MUX 2
176
PASS THROUGH VIDEO
MUX 1
DIGITAL VIDEO
820
822
ANALOG VIDEO
168

FIG. 27

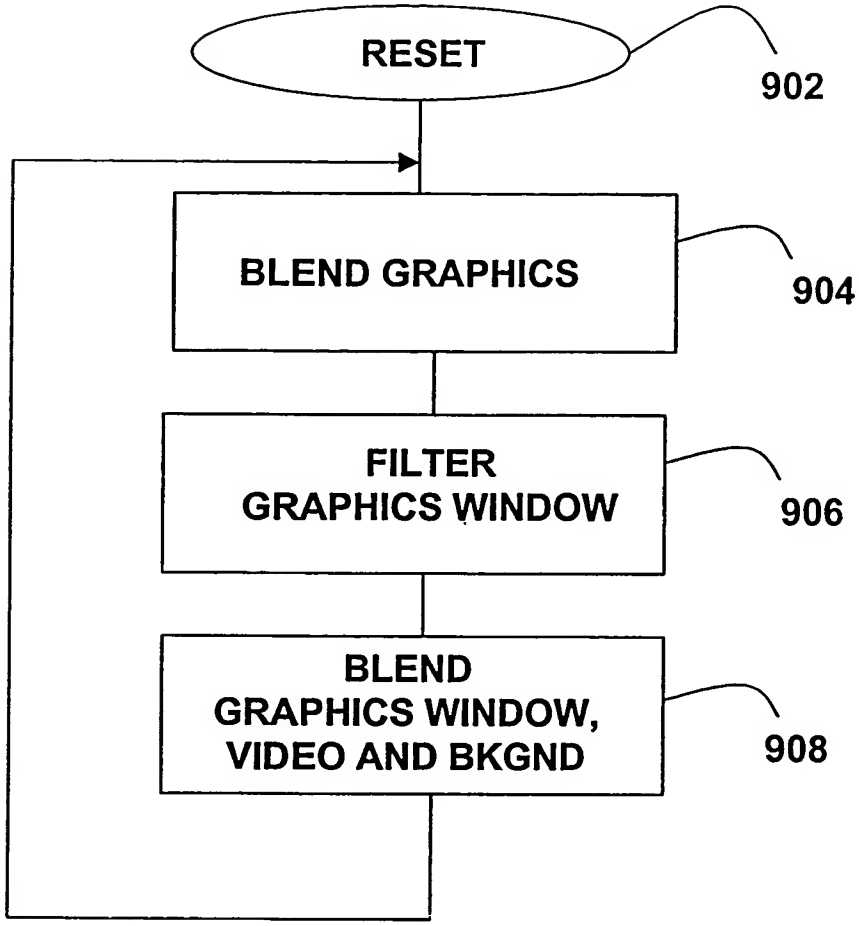
RESET
902
BLEND GRAPHICS
904
FILTER GRAPHICS WINDOW
906
BLEND GRAPHICS WINDOW, VIDEO AND BKGND
908

FIG. 28

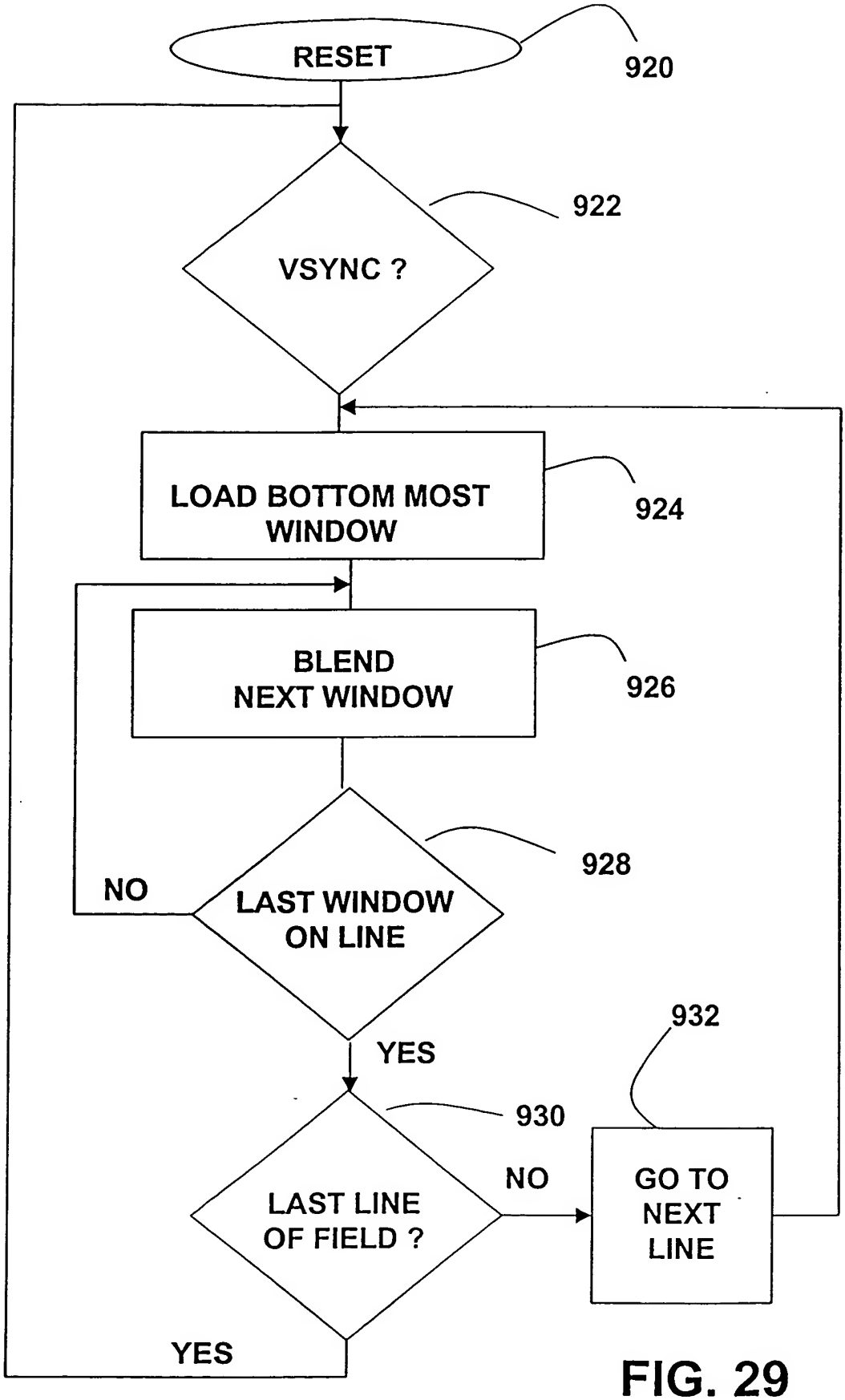
RESET
920
VSYNC ?
922
LOAD BOTTOM MOST WINDOW
924
BLEND NEXT WINDOW
926
LAST WINDOW ON LINE
928
NO
YES
LAST LINE OF FIELD ?
930
NO
GO TO NEXT LINE
932
YES

FIG. 29

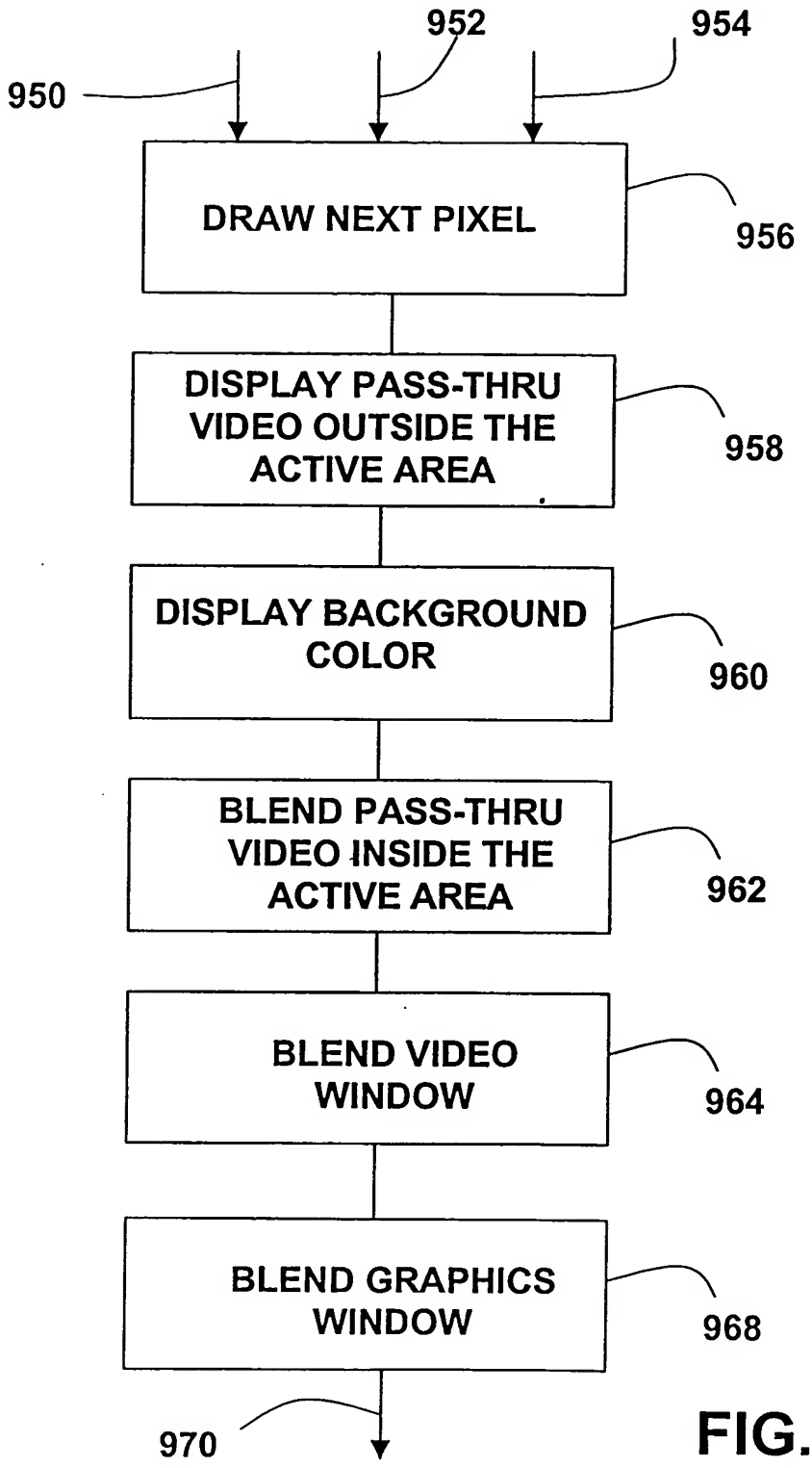
950
952
954
DRAW NEXT PIXEL
956
DISPLAY PASS-THRU VIDEO OUTSIDE THE ACTIVE AREA
958
DISPLAY BACKGROUND COLOR
960
BLEND PASS-THRU VIDEO INSIDE THE ACTIVE AREA
962
BLEND VIDEO WINDOW
964
BLEND GRAPHICS WINDOW
968
970

FIG. 30

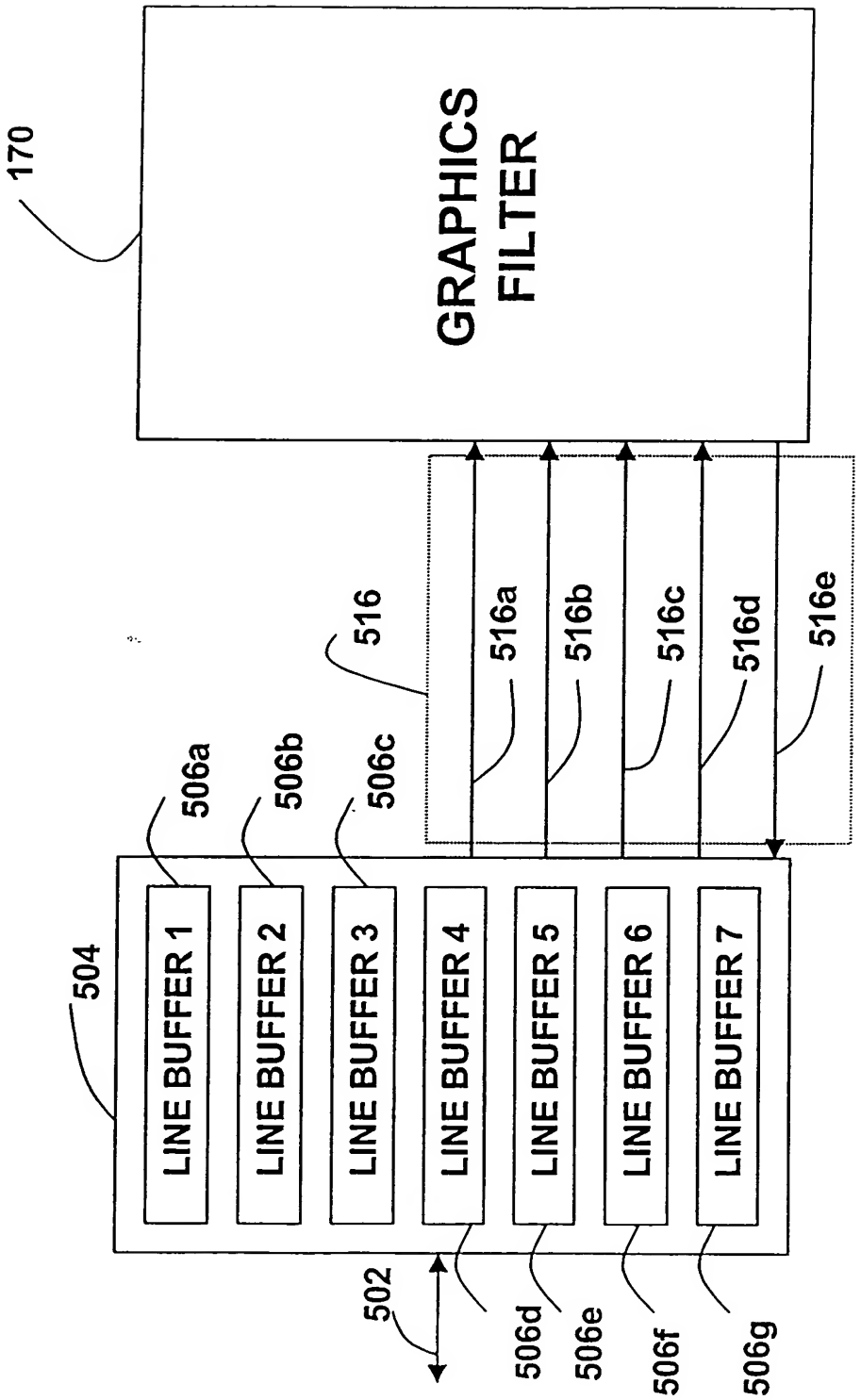
170
GRAPHICS FILTER
516
516a
516b
516c
516d
516e
506a
506b
506c
504
LINE BUFFER 1
LINE BUFFER 2
LINE BUFFER 3
LINE BUFFER 4
LINE BUFFER 5
LINE BUFFER 6
LINE BUFFER 7
502
506d
506e
506f
506g

FIG. 31

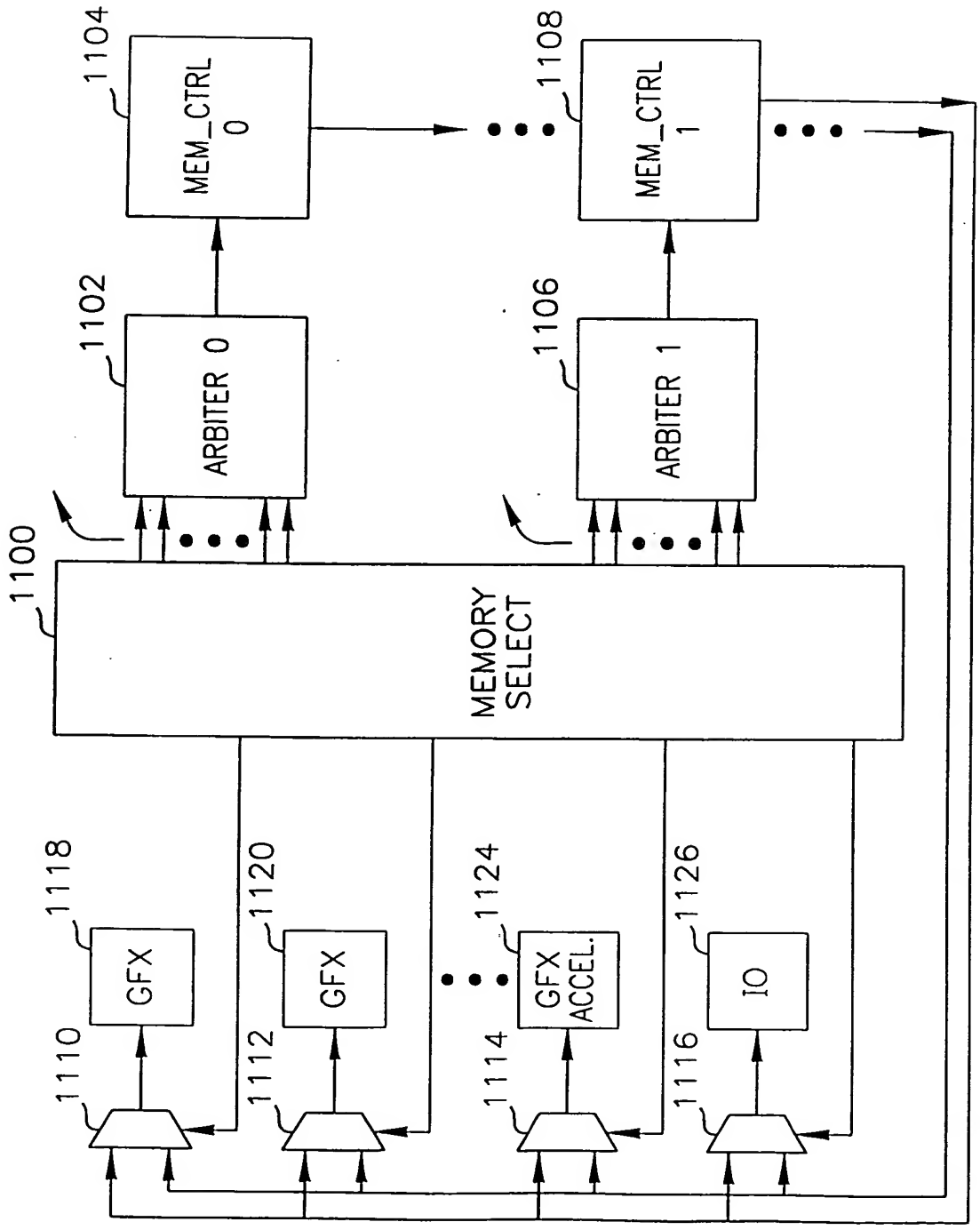
1104
MEM_CTRL 0
1108
MEM_CTRL 1
1102
ARBITER 0
1106
ARBITER 1
1100
MEMORY SELECT
1118
GFX
1120
GFX
1124
GFX ACCEL.
1126
IO
1110
1112
1114
1116

FIG. 32

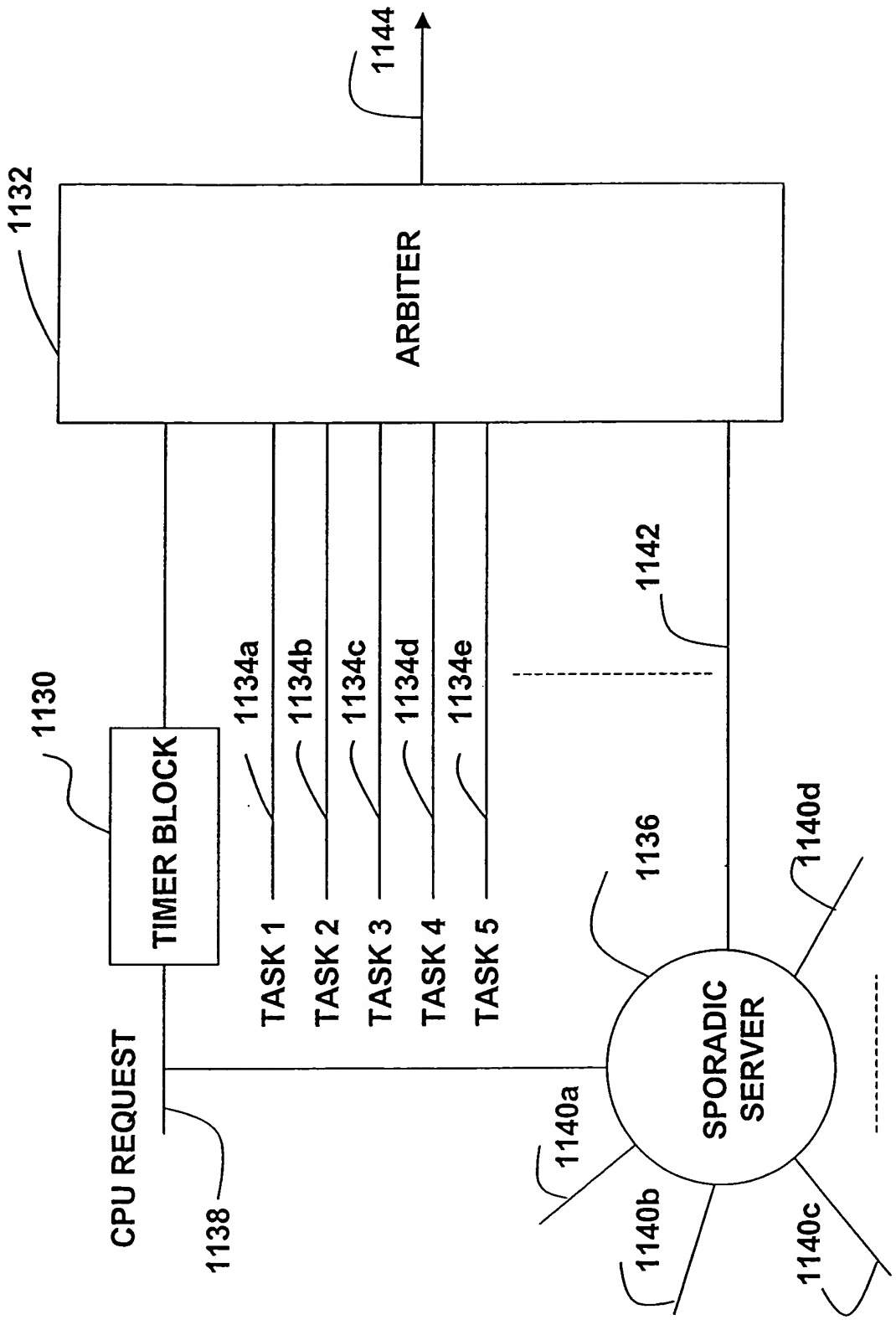
1144
1132
ARBITER
1142
1130
TIMER BLOCK
1134a
1134b
1134c
1134d
1134e
TASK 1
TASK 2
TASK 3
TASK 4
TASK 5
1136
1140d
CPU REQUEST
1138
SPORADIC SERVER
1140a
1140b
1140c
LOW PRIORITY TASKS IN ROUND ROBIN

FIG. 33

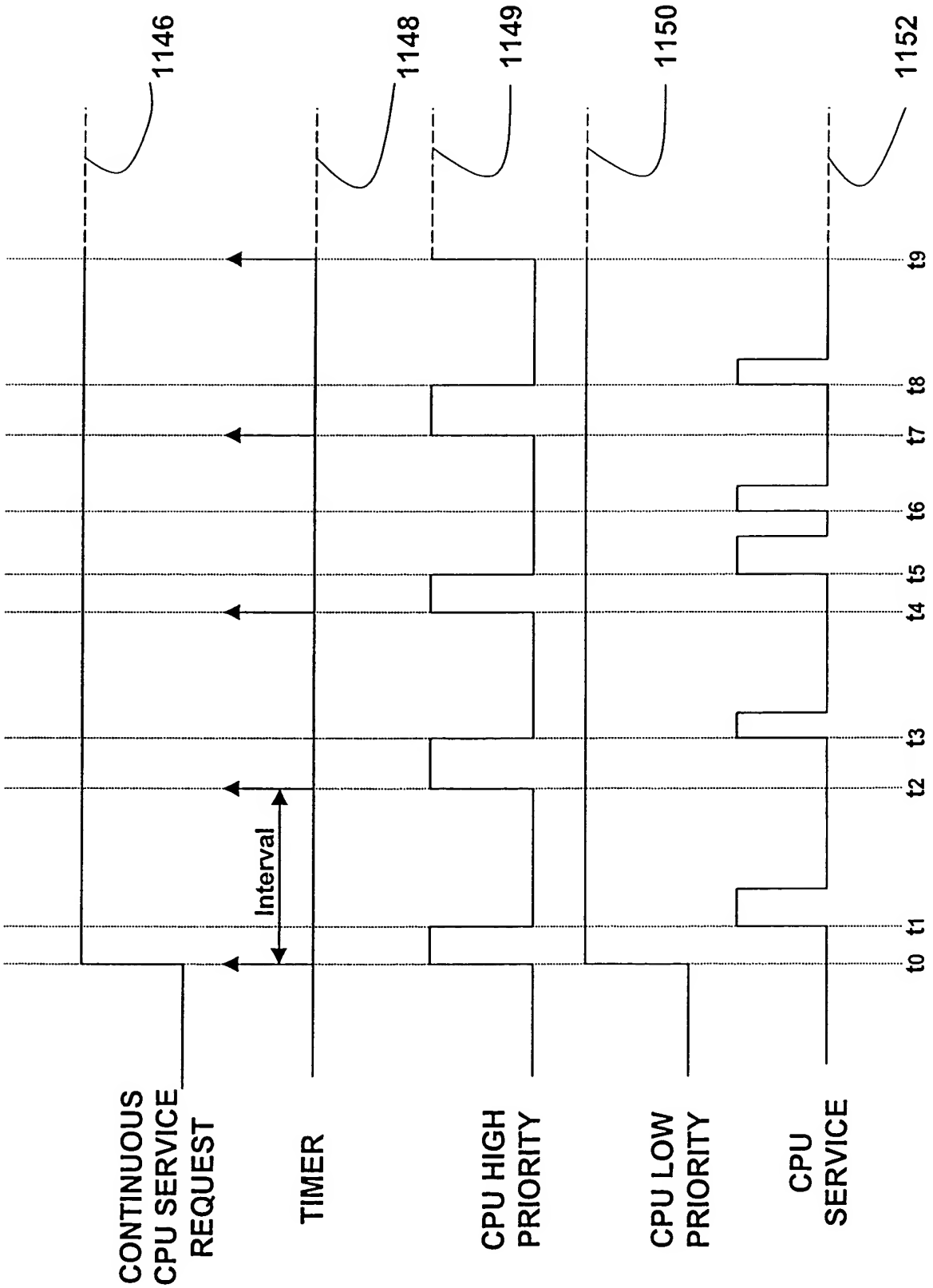
1146
1148
1149
1150
1152
t9
t8
t7
t6
t5
t4
t3
t2
t1
t0
Interval
CONTINUOUS CPU SERVICE REQUEST
TIMER
CPU HIGH PRIORITY
CPU LOW PRIORITY
CPU SERVICE

FIG. 34

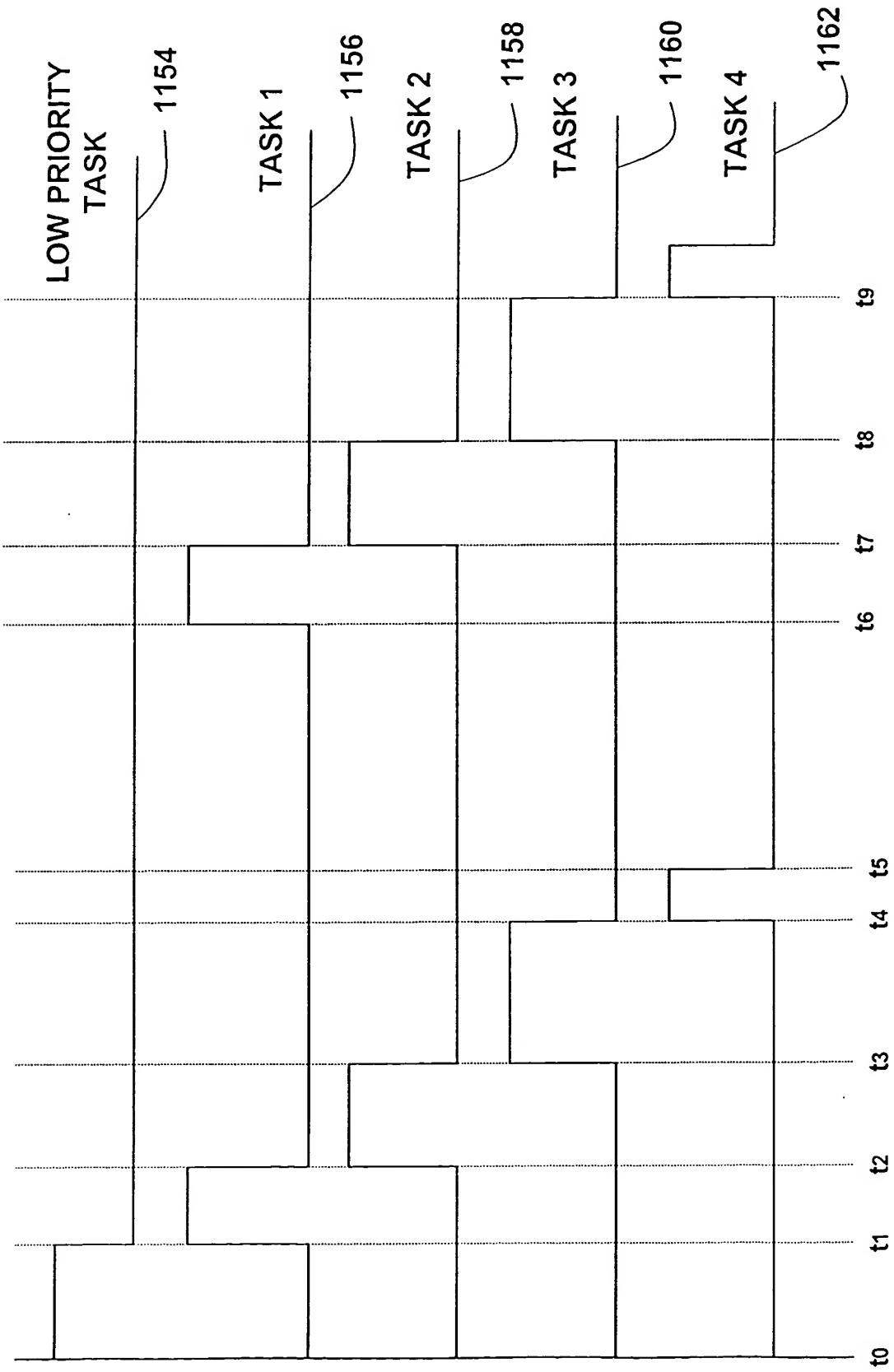
LOW PRIORITY TASK
1154
TASK 1
1156
TASK 2
1158
TASK 3
1160
TASK 4
1162
t9
t8
t7
t6
t5
t4
t3
t2
t1
t0

FIG. 35

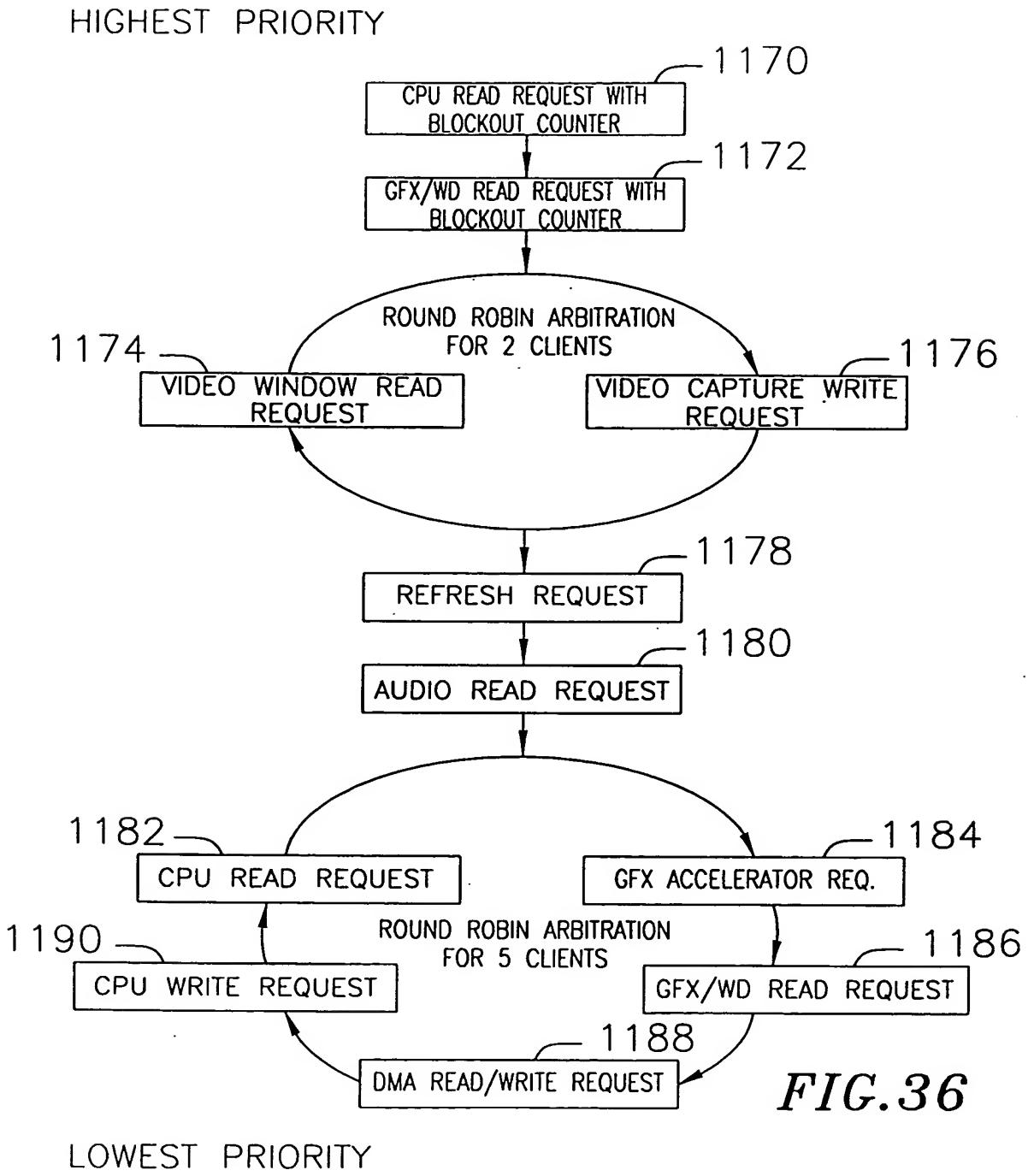
HIGHEST PRIORITY
1170
CPU READ REQUEST WITH BLOCKOUT COUNTER
1172
GFX/WD READ REQUEST WITH BLOCKOUT COUNTER
ROUND ROBIN ARBITRATION FOR 2 CLIENTS
1174
VIDEO WINDOW READ REQUEST
1176
VIDEO CAPTURE WRITE REQUEST
1178
REFRESH REQUEST
1180
AUDIO READ REQUEST
1182
CPU READ REQUEST
1184
GFX ACCELERATOR REQ.
ROUND ROBIN ARBITRATION FOR 5 CLIENTS
1190
CPU WRITE REQUEST
1186
GFX/WD READ REQUEST
1188
DMA READ/WRITE REQUEST
LOWEST PRIORITY

FIG.36

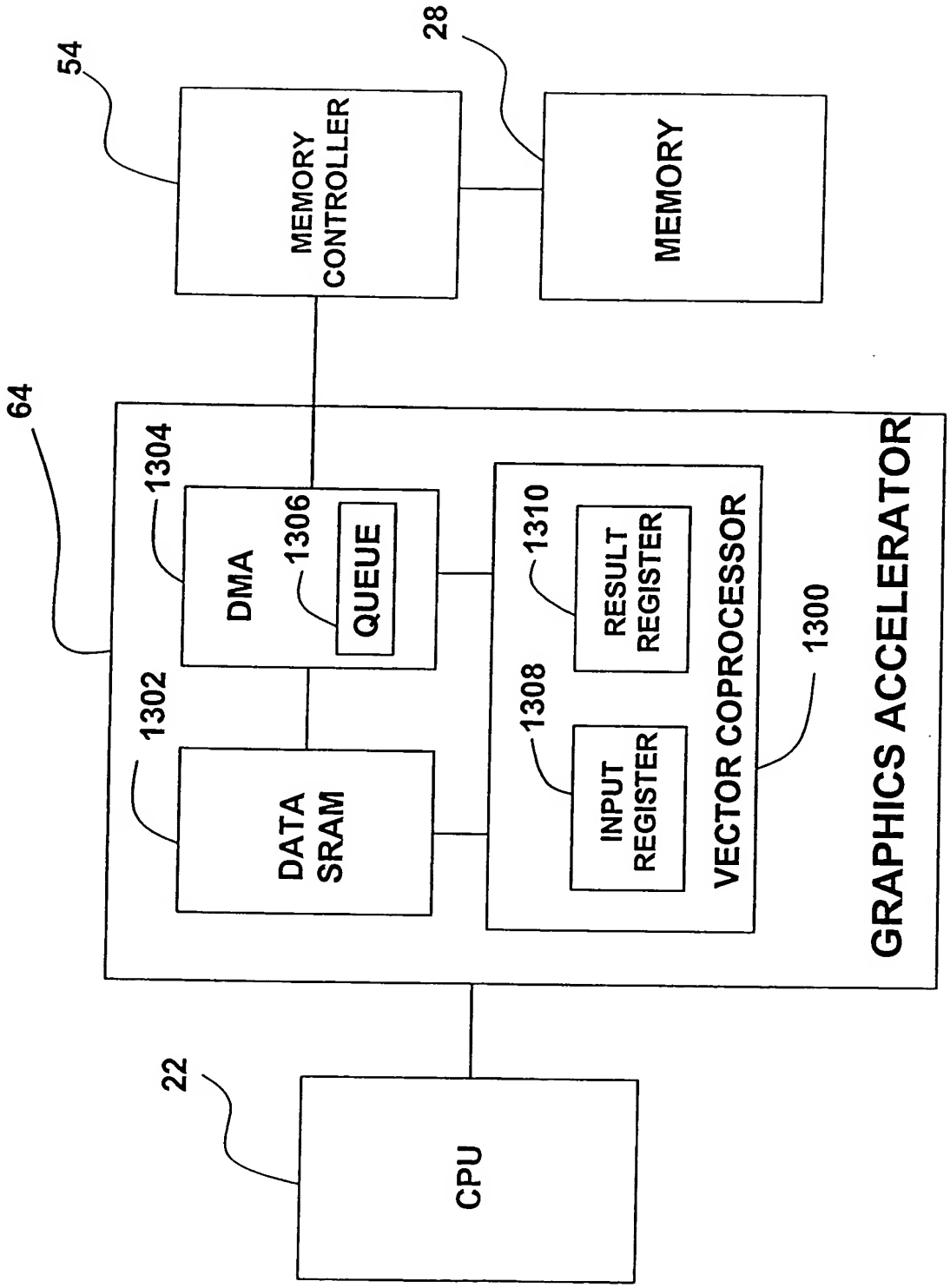
54
28
MEMORY CONTROLLER
MEMORY
64
1304
DMA
1306
QUEUE
1310
RESULT REGISTER
1308
INPUT REGISTER
VECTOR COPROCESSOR
1300
1302
DATA SRAM
GRAPHICS ACCELERATOR
22
CPU

FIG. 37